SOME NOTES ON THE PROPOSED DESIGN OF THE ZEUS-MVD CLOCK & CONTROL

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The main functions of the C&C MASTER are to receive the standard GFLT information and pass them onto the C&C SLAVES, decode the trigger information to produce and send the "TRIG IN" and "FCS TP" signals to the HELIX INTERFACE MODULE, together with correctly timed 96nsec "RCLK", and to handle the "ERROR (RESET REQ.)", "FATAL ERROR" and "BUSY" signals from the ADCs (via the C&C SLAVES) to produce "BUSY" and "FATAL ERROR" returns to the GFLT and "NOT RESET" to the HELIX INTERFACE MODULE.

It allows a continuous VME read access to registers with all the relevant signals being received from the ADCs (via the C&C SLAVES) and sent back to the GFLT.

Additionally, the C&C MASTER is able to operate in a stand-alone mode for test purposes, generating its own 96nsec clock and able to accept all the relevant GFLT-type information and commands via the VME.

The C&C SLAVE receives all the GFLT signals from the C&C MASTER and distributes them to all the ADCs within its crate via the User Defined Pins of the VME P2 or P3 connector as TTL bus, receiving back the "BUSY" and the two "ERROR" lines as wire-OR from the ADCs.

It distributes the suitably timed 96nsec "RCLOCK" synchronously to all the ADCs within its crate, via a specially wired-in set of 20 twisted pairs of identical length, either to two dedicated User Pins on each backplane connector, or to front-panel connectors.

The C&C SLAVE also allows a continuous VME read access to a register with the three ADC-produced signals.

Additionally, the C&C SLAVE can operate in a stand-alone mode for test purposes, receiving these three ADC-produced-type signals via the VME.

FOR THE FOLLOWING NOTES, PLEASE REFER TO THESE DIAGRAMS

- Internal connections for Master
- Internal connections for Slave
- State diagram for Master
- State diagram for Slave
- Registers for Master
- Registers for Slave

- 1) As proposed, the C&C MASTER is a single, 9U, VME card. It receives the GFLT signals on four 34-pin IDCs as ECL pairs, and distributes them up to four C&C SLAVES via four identical sets of 34-pin IDCs. (Assuming the need of up to 256 readout cells, and 8 ADCs on each ADC module, we only need 32 ADC modules, ie. only two VME crates. But with only four ADCs on each ADC module, four VME crates may be required. Therefore I propose to allow for four sets of C&C SLAVES in this preliminary design.)

- 2) The C&C SLAVES are connected to the master via four sets of ribbon cables of identical length, allowing for the carrying of the "CLOCK" and the returning "BUSY" and two "ERROR" lines. (The alternative method would be to daisy-chain all the signals on one set of cables - apart of the clock -, which is perfectly feasible if the length is kept to about 1m for each 'daisy-chain-link'. The clock would have to be distributed separately via a set of cables of identical length. The whole daisy chain would also have to be terminated separately at the last link of the chain. I believe the first method above to be easier to implement and and to be more flexible.)

- 3) The optical connection to the HELIX INTERFACE MODULE is via a commercially available optical ribbon cable & connector.

- 4) There are 4 registers on the C&C MASTER to allow for VME-write/read access when in the LOCAL MODE (ie. stand-alone and/or test) to generate all the GFLT-type signals and returns. They are VME-read-only while in the GFLT MODE (ie. running).

- 5) Further 2 registers allow continuous VME-write/read access for a) Command Reg. to set C&C MASTER to LOCAL or GFLT Control, and overall "RESET" b) Mask Reg. to enable masking-off of the returns from the C&C SLAVES

- 6) Final 2 registers allow VME-read-only access to the four sets of the three returns from each C&C SLAVE, and to the four signals sent to the HELIX INTERFACE MODULE with the current C&C MASTER state.

- 7) The GFLT signals are all latched on the C&C MASTER by a suitably delayed 96nsec GFLT "CLOCK"

- 8) The three signals sent to the HELIX INTERFACE MODULE are also latched on this board by a suitably delayed 96nsec "RCLOCK" .

- 9) There are only 3 registers on the C&C SLAVE, one for the three returns from ADCs (VME-read-only in GFLT MODE, VME-write/read in the LOCAL MODE), one VME-write/read to set the MODE and RESET, and one VME-read-only for the current C&C SLAVE state.

- 10) All the GFLT signals to and from the C&C MASTER are latched on the C&C SLAVE as well.

- 11) The simple "state diagram" of the C&C MASTER also shows the proposed handling of the "BUSY" and "ERROR (RESET REQ.)" signals by the C&C MASTER.

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