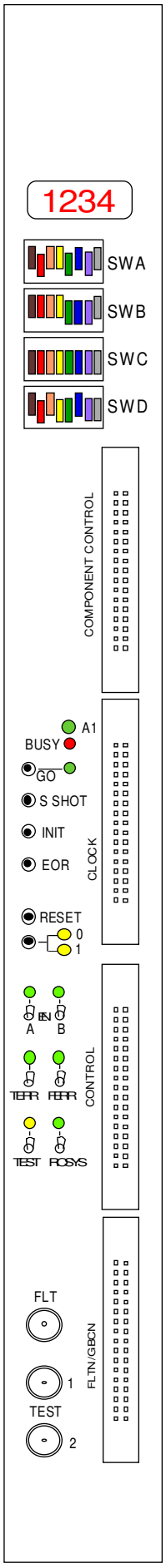

ZEUS GFLT SIMULATOR

PCB Version

v1.0

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1. INTRODUCTION

The GFLT SIMULATOR (GS) was designed to allow ZEUS Components to be connected either to the GLOBAL FIRST LEVEL TRIGGER (GFLT) or to a TEST CIRCUIT, without changing the cabling. The GS includes the TEST CIRCUIT, which allows simple stand-alone testing of Component operation. The GS was first produced as a wire-wrap circuit, and a number of slightly different versions were made. This note describes the printed circuit version only.
The GS is entirely manually operated, by means of front-panel switches. The only connections to the backplane are for power.

2. Basics

The basic scheme is shown in fig. 2
It is essentially a 2-way multiplexer, connecting up to 2 components either to the GFLT or to the TEST CIRCUIT.
The GS has no connection to the crate backplane except for power (2.5A at +5V and 2A at -5.2V , both fused) and all control is by means of manually operated switches. Status is indicated by a 4 character alphanumeric led display, together with 11 individual front-panel leds.
When in GFLT mode the module is transparent to signals from the GFLT, apart fromadding a delay to each signal of approximately 12 nS. In TEST mode the TEST CIRCUIT can generate CLOCK, BCN0, FLTACCEPT, FLTN / GBCN in various modes controlled by switches. There are some differences in the functionality required by the FDET compared with that required by the CTD; only one version has been produced with the selection of functionality being made by a jumper (LK1) on the printed circuit board. There is no front-panel indication of the state of this link; the user must ensure that it is not present for CTD mode and present for FDET mode.

2.1. *Connection to GFLT and Components*

fig. 3 shows the connector layout . The four front-panel mounted 34-way idc connectors are used to connect to the GFLT, the 5 mounted on the printed circuit board are used to connect to the components. Of these 5 connectors the bottom 3 carry signals to the component (GFLT NUMBER CABLE, GFLT CONTROL CABLE,GFLT CLOCK CABLE) and the remaining pair (side by side) are used to connect the COMPONENT CONTROL CABLE from up to 2 components. In CTD mode, only the connector marked Component A in fig 3 is active. In FDET mode both connectors function identically.

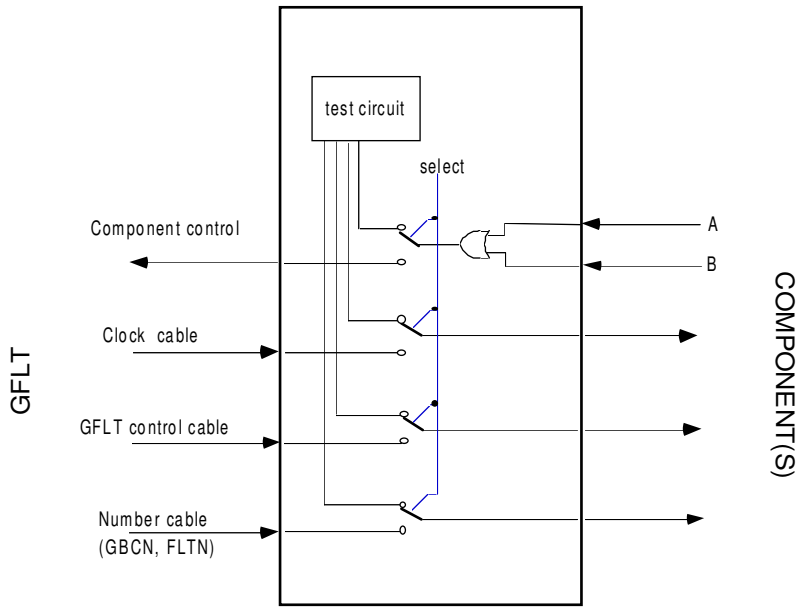


fig 2

2.2. *DIL Switches*

fig 4 indicates the nomenclature for the 4 front-panel mounted DIL switches. When a group of switches eg SWA(2:7) is referred to, the rightmost switch is the least significant and has a value of 0 or 1. The next switch has a value 0 or 2 and so on.

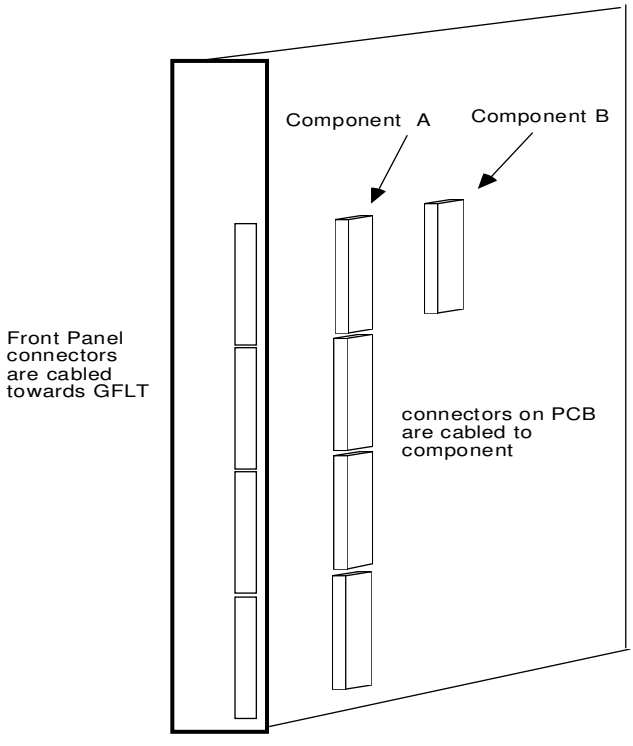


fig 3

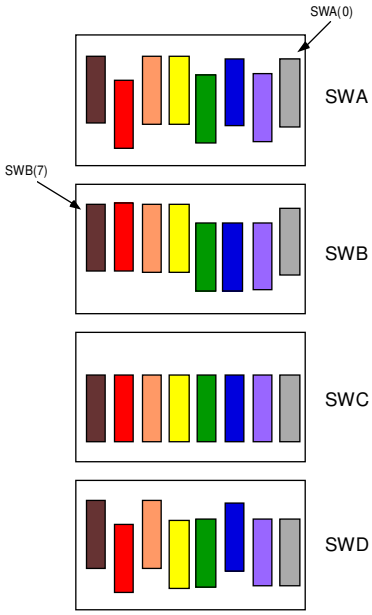


fig 4

3. GFLT Mode

This mode is selected by setting SWA(0) to ***DOWN***. The mode is indicated by the alphanumeric display showing **GFLT** .

3.1. *Signals from GFLT to Component*

In this mode all signals from the GFLT are routed directly to the component. From the NUMBER CABLE 16 signals are received, FLTN(0:7) AND GBCN(0:7). From the GFLT Control Cable 13 signals are received, ACCPTFLG, ABRTFLG, ROUSR(0:2),ROAMB(0:1),ROSYS(0:1), TTYPE(0:2) and TESTENBL. From the Clock Cable 4 signals are received, CLOCK, BCN0, pEMPTY and eEMPTY. All received signals are terminated by 120 ohm resistors. All output lines are pulled down with 390 ohm resistors on each line.

3.2. *Signals from Component to GFLT*

3 signals are received from the component, BUSY, FERR and TERR. These signals are treated differently depending on the presence or not of jumper LK1. This jumper is located on the printed circuit board and if absent the board is in CTD mode, if present it is in FDET mode.

3.3. *CTD Mode*

In CTD mode only the signals (BUSY, TERR, FERR) from the connector COMPONENT A (see fig 3) are used, the signals from COMPONENT B are ignored. All three signals are passed directly to the output connector (the Component Control Cable, towards the GFLT). The CLOCK received from the GFLT is returned to it as the component signal **T-mark**. Note that in this mode the front-panel switches ENA ,ENB, TERR and FERR have no effect and the corresponding leds have no significance.

3.4. *FDET Mode*

The GS is in FDET mode when LK1 is present. This link can be made by a jumper or by a wire-wrap link.
All signals from the GFLT are passed to the components as in CTD mode, the only difference is in the way the signals from the components are handled.
The signals from the components are BUSY, FERR and TERR. They are controlled by the front-panel toggle switches marked ENA, ENB, TERR and FERR.
The effect of these switches is shown in fig 6.

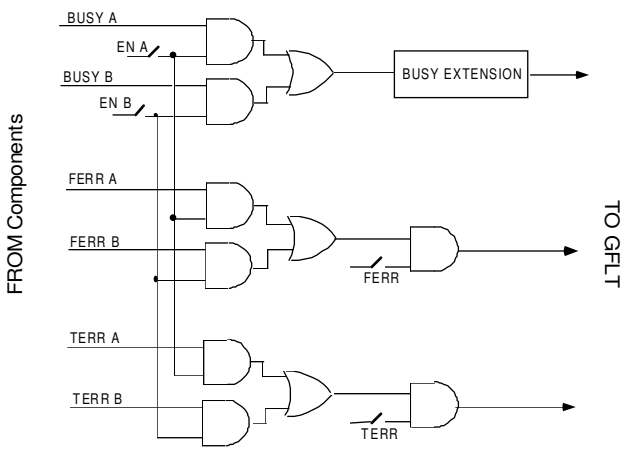


fig 6

If EN A or EN B is in the off position (LED off) then no signal from that component is transmitted to the GFLT. FERR and TERR can be disabled

3.4.1. BUSY Extension

The OR of the BUSY A and BUSY B signals is applied to a circuit which extends the busy signal by a time controlled by SWE, an 8-way dil switch mounted on the printed circuit board. The Busy Extension Circuit is essentially a counter, clocked by the 96-nS clock. When neither of the OR'd Busy signals are asserted, the clock is held loaded with the value set on SWE(0:7) The OR circuit intrduces an additional delay to the BUSY signal output to the GFLT of aproximately 10 nS. At the trailing edge of BUSY A OR BUSY B the counter starts counting down and the BUSY output is maintained asserted until the counter reaches zero. The SWE switches have a value of 1 when *up*.

4. TEST Mode

TEST Mode is selected by setting SWA(0) to **UP**. In TEST mode the components are disconnected from the GFLT, ie all signals *from* the GFLT are ignored and all signals *to* the GFLT are set to zero. In this mode the TEST Circuit can generate the signals normally generated by the GFLT, controlled by the front panel switches. When this mode is entered the alphanumeric display will show all zeroes, and unless the display mode is changed will display the least significant 4 digits of a 6-digit decimal counter which counts FLTACCPTs.

4.1. *FLTACCPT*

The main function of the Test Circuit is to generate FLTACCPT pulses.
These can be generated as single-shot or continuous, periodic or random. Single-shot pulses can be NORMAL, INIT or EOR. In all cases the circuit obeys the busy signal from the Component and outputs FLTACCEPTs only when BUSY is not asserted. fig 7 shows the main features of the FLTACCPT generator circuit (much simplified).
In the inactive state the DELAY COUNTER is held loaded with the state of SWB(0:5) and the WIDTH COUNTER is held loaded with the state of SWA(2:7) When RUN is asserted by pressing one of the switches GO (continuous normal FLTACCPTs), Single-Shot, INIT or EOR the delay counter counts up. When it reaches the end of count (all 1s) a flip-flop (REQUEST) is set. When BUSY is not asserted the REQUEST causes the FLTACCEPT to be set and the WIDTH counter starts counting up. When it reaches full count FLTACCPT , REQUEST and the single-shot flags are cleared. The counters are reloaded with the switch states. If GO is asserted the process is repeated, otherwise the circuit waits for one of the 4 RUN switches to be pressed.

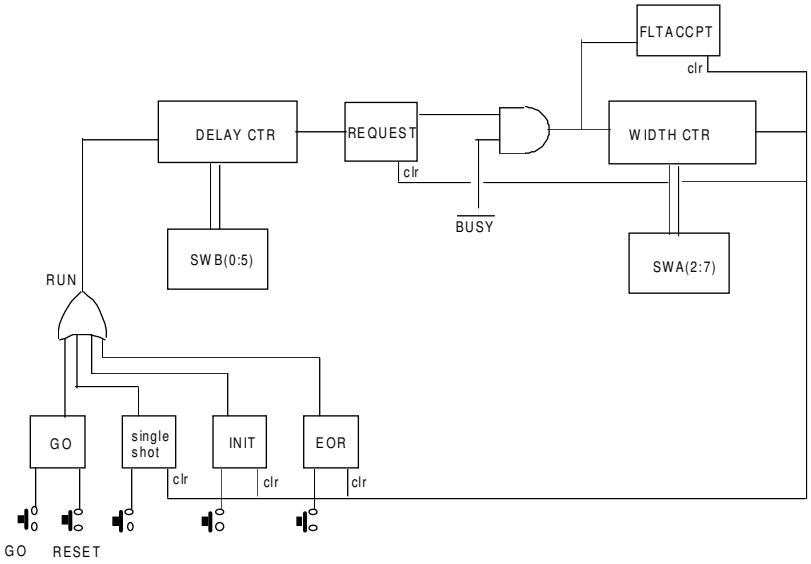


fig 7

4.1.1. Width of FLTACCPT

The width of the FLTACCPT pulse is controlled by SWA(2:7)
Minimum width is 2* 96 nS, ie 2 counts of the internally generated 96 nS clock (10.42 Mhz)
Width is (2 + 2*n) * 96 nS where n is the value of SWA(2:7). SWA(2) has the value 1 when **UP**, SWA(3) has the value 2 when **UP** and so on to SWA(7) which has the value 32 when **UP**.

4.1.2. Rate of FLTACCPT

The rate of FLTACCPPT is controlled by the component by asserting BUSY. Here it is assumed that BUSY is not asserted, in which case the FLTACCPT rate is governed by the combination of the DELAY counter and the WIDTH counter. The Width counter gives a maximum width of (2 + 2*63) * 96 nS or 12.3 µS. This means that for most practical purposes the rate is set by the DELAY Counter. The delay counter is loaded with a number selected by SWB(0:5). These 64 possible numbers are in fact 24-bit numbers which are stored in PROMs, SWA(0:5) providing a 6-bit address to the PROMs. The selected delay can be any number in the 24-bit range and so the delay can be in the range 0 to 1.6 seconds, giving a range of rates from approximately 0.6 Hz to 2 Mhz. But only 64 rates can be programmed since they have to be selectable by SWB(0:5). The following table gives the rates which have been programmed. Note that the PROMS are re-programmable but this must be done outside the GS.
SWB(0) is the least significant and 1 is **UP**.

switch value	rate (Hz)	switch value	rate (Hz)	switch value	rate (Hz)
63	1	41	90	20	1000
62	2	40	100	19	1100

61	3	39	120	18	1200
60	4	38	140	17	1300
59	5	37	160	16	1400
58	6	36	180	15	1500
57	7	35	200	14	1700
56	8	34	230	13	1800
55	9	33	260	12	1900
54	10	32	300	11	2000
53	12	31	350	10	2200
52	14	30	400	9	2400
51	17	29	450	8	2600
50	20	28	500	7	2800
49	25	27	550	6	3000
48	30	26	600	5	3500
47	35	25	650	4	4000
46	40	24	700	3	4500
45	50	23	750	2	5000
44	60	22	800	1	6000
43	70	21	900	0	7000

4.1.3. Periodic and Random FLTACCPTs

fig 8 shows a more expanded view of the circuit which provides the PROM address. There are 2 sources of address, SWB(0:6) and an 11 bit counter which is incremented by FLTACCPT. The source selection is made by SWB(7).

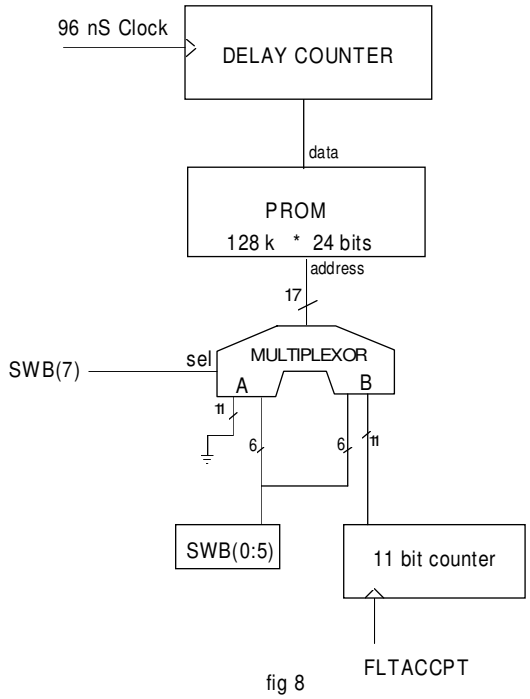


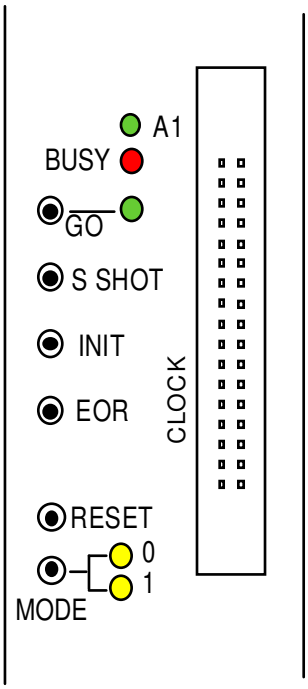
fig 8

When this switch is **DOWN** then the 17-bit address required by the PROMS is made up as follows: 11 most significant bits are set to zero, and the least significant 6 bits are provided by SWB(0:5). In this case the delay is the fixed number selected by SWB(0:5) and the FLTACCPTs occur (if BUSY is not asserted) in a periodic fashion.

If SWB(7) is **UP** then the 6 most significant bits of the address are provided by SWB(0:5) and the least significant 11 bits are provided by the 11-bit FLTACCEPT counter. In other words the PROMS are divided into 2k pages (24 bits wide), *one* of which is selected by the switches. After each FLTACCPT the counter is incremented, thus addressing a new word from the selected 2k page of the PROM. This word provides the delay for the *next* FLTACCEPT. Each page of the PROMS has been programmed with "random" values to give a mean rate (with BUSY not asserted) approximately equal to the rate which is provided by SWB(0:5) if PERIODIC mode is selected by setting SWB(7) down. Note that there are 64 pages in the PROMs but one of these is used for the PERIODIC values, page 0. This page should therefore not be selected when RANDOM mode is selected.

4.2. Control Push-Button Switches

FLTACCEPTs are generated by pressing one of 4 push-button switches on the front panel, these are marked **GO**, **S_SHOT**, **INIT** and **EOR**. Associated with these is another push-button marked **RESET**.



4.2.1. GO

Pressing this causes the flip-flop GO to be set (fig 7) and FLTACCPTs will be generated until RESET is pressed.
The state of the GO flip-flop is indicated by a LED.

4.2.2. S_SHOT, INIT and EOR

If one of these is pressed while the GO led is *not* lit, a single FLTACCPT is generated. If the GO led is lit, these switches have no effect.

4.3. *Signals sent with FLTACCPT in Test Mode*

All lines specified in the GFLT Design Document I (v 5.1) with the exception of 24 nS CLK, are driven.
Of the Clock Cable signals, eEMPTYB and pEMPTYB are permanemtly unasserted in test mode.
Of the GFLT Control Cable signals, ABRTFLG, ROAMB0 and ROAMB1 are permanently unasserted in test mode.

4.3.1. ROUSR,ROSYS

The following table shows the relationship of these 5 signals with trigger type.

TYPE	ROUSR2	ROUSR1	ROUSR0	ROSYS1	ROSYS0
NORMAL	0	0	0	0	0
INIT	1	0	0	1	0
EOR	1	1	1	1	0

4.3.2. TTYPE(2:0)

These signals will be described later under “TEST ENABLE”

4.3.3. GBCN(7:0)

Global Bunch Crossing Number is essentially the state of a free-running 8 bit counter, counting between 0 and 219, and latched by fltaccpt. It is static during the interval between FLTACCPTs and obeys (as do all signals) the setup and hold times as specified in the Design Document.
BCN0 is generated by the same 8-bit counter.

4.*3.3.1.Fixed GBCN*

As a diagnostic facility FLTACCPTs may be generated at times such that GBCN(7:0) will always have the same value. This facility is enabled by setting SWA1 to ***down.*** The state of SWA1 is indicated by the front panel LED A1.The value of GBCN will be the same as that of SWC(7:0). Note that in this mode SWC is **1 = down, 0 = up**. In the figure shown here SWC has a value 72 decimal.
The correct relationship to BCN0 is maintained. Note that, if the fixed GBCN mode is selected, SWC(7:0) must be set to a value not exceeding 219, otherwise no FLTACCPTs can be generated.

4.3.4. FLTN(7:0)

First Level Trigger Number is an 8 bit count of FLTACCPTs.
It is cleared by INIT or by RESET. It is incremented by FLTACCPTs other than INIT, including EOR.

4.*4. The Front Panel AlphaNumeric Display*

This 4-character display indicates one of 4 items in Test Mode.

1. The least significant 4 digits of an FLTACCPT 6-digit decimal counter. This counter is *not* the FLTN counter, and counts all FLTACCPTs including init. It is cleared when Test Mode is entered, or by RESET. This display mode is indicated by the 2 ***mode*** leds showing both **on**.
2. The most significant 4 digits of the FLTACCPT decimal counter. This mode is indicated by *one* of the ***mode*** leds being **on**.

3. The FLTN. The display shows TNXX where XX is FLTN(7:0) in hex. Both mode leds are unlit.
4. The GBCN. The display shows BCXX where XX is GBCN(7:0) in hex. Both mode leds are unlit.

The different display modes are selected by pressing the MODE pushbutton switch, each press takes the display into the next mode, wrapping around.

4.5. TESTENABLE

The GS implements the TESTENBL system and in addition provides a variable-timed pre-FLTACCPT pulse. TESTENBL mode is selected by the TEST front-panel toggle switch. When this mode is selected the associated led is lit. In TESTENBL mode the TESTENBL signal on the GFLT Control Cable is asserted for 96 nS, 1 clock period, 22000 clock periods before the FLTACCEPT. ROSYS1 is asserted when TESTENBL is asserted and remains asserted until the end of the associated FLTACCPT. Note that the frequency of the FLTACCEPTs must be such that there are at least 22000 clock periods between the end of one FLTACCEPT and the beginning of the next. For this reason TESTENABLE mode should not be used when "random" mode is also selected.

4.5.1. Test Pre-Pulse

The Test Pre-Pulse is a pulse which is issued a programmable time before the FLTACCEPT when TESTENBL mode is selected. This time is selectable as follows. SWC(0:6) is used o set the pre-pulse time in units of 96 nS, ie from 0 to 12.192 μS. Note that SWC is also used for the "fixed GBCN" test mode: simplest not to use these modes together!) The test pre-pulse time is now delayed (relative to FLTACCEPT) in up to 3 steps of 24 nS each ie 0 to 72 nS. This delay is controlled by SWD (5:6). Finally a further delay of 0 to 31 nS in steps of 1 nS is made by SWD (0:4). By these means the pre-pulse can be set 0 to 12 μS in 1 nS steps. The pre-pulse may be used, if required, to trigger a calibrate signal. 2 copies of the pre-pulse are available at NIM levels at Lemo sockets. For convenience in scoping a copy of FLTACCPT is also available as a NIM output. For flexibility the polarity of the pre-pulse and the FLTACCPT are independently selectable by means of jumpers at LK3 and LK2 respectively.

5. Questions or Problem Reports

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