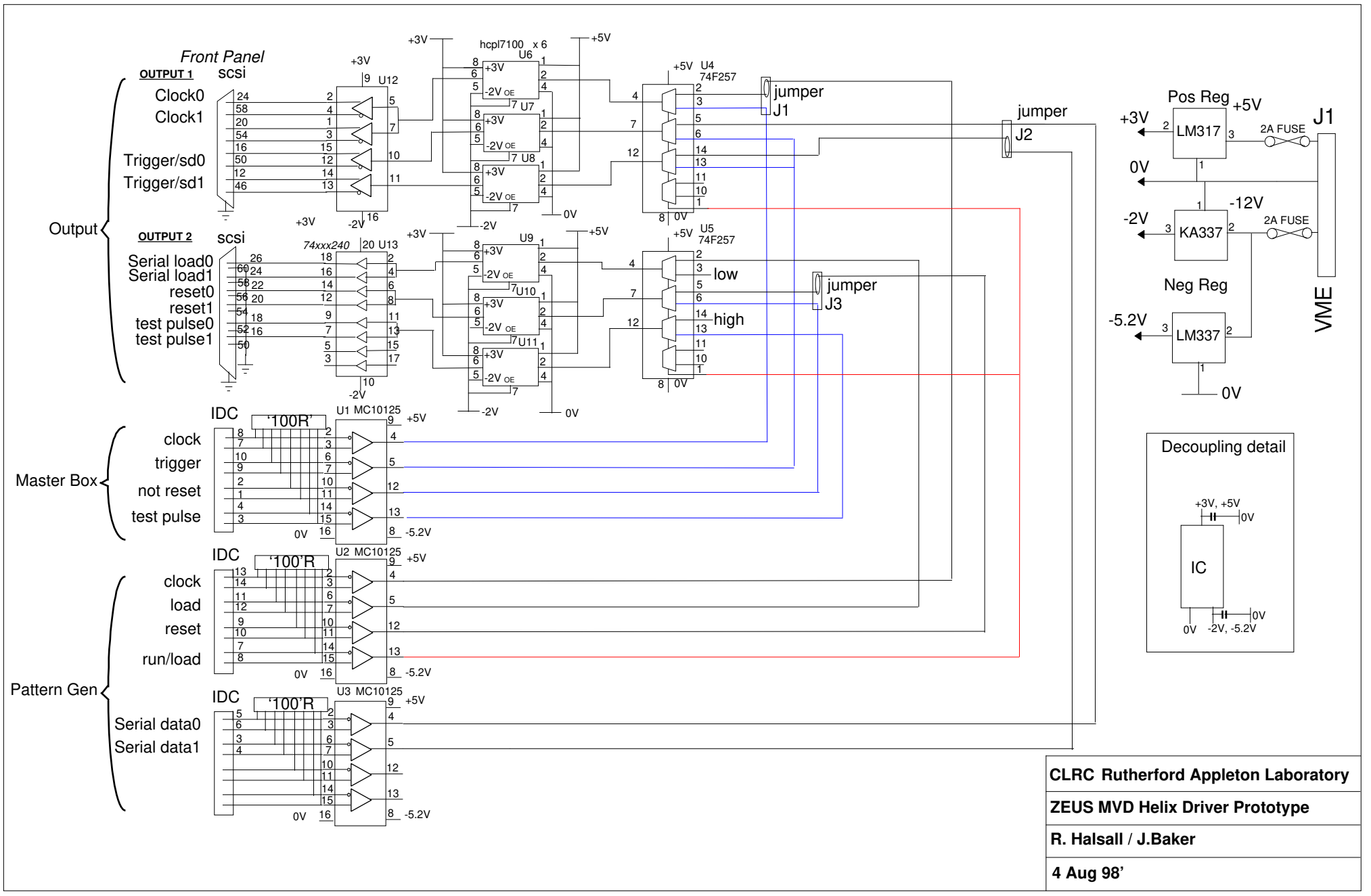
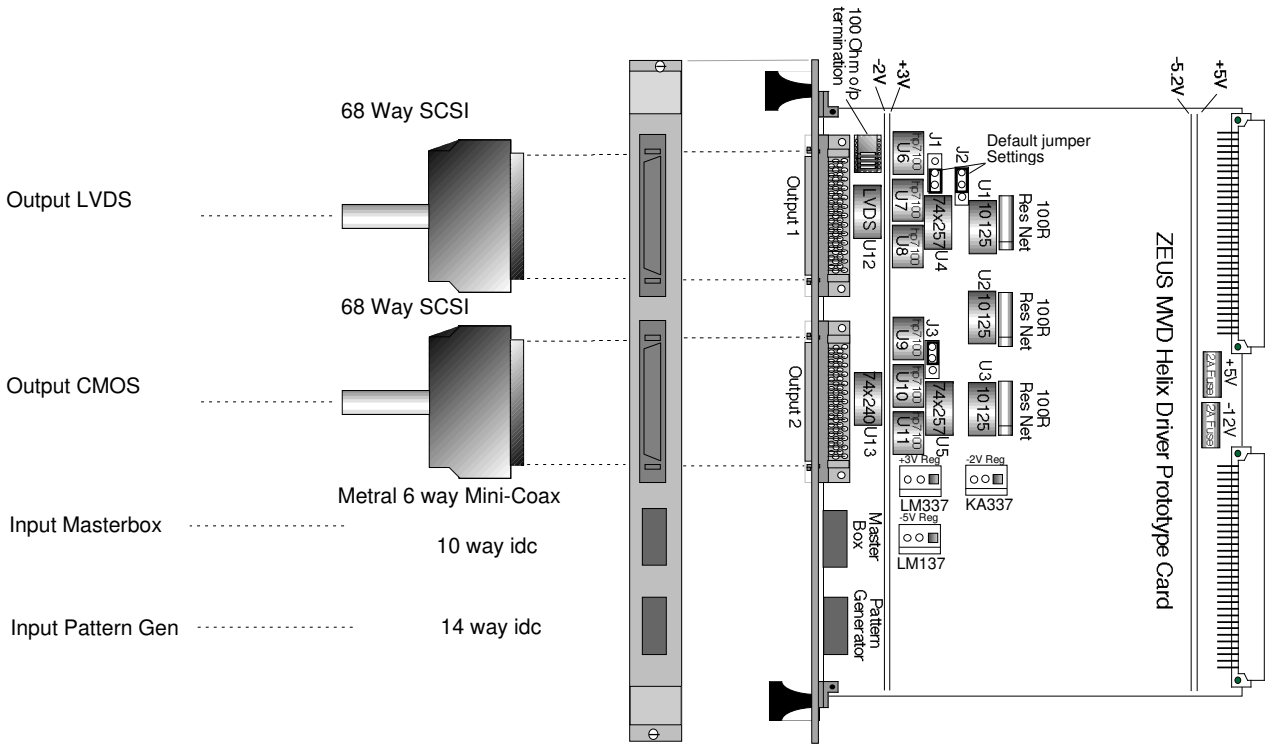

Front Panel
OUTPUT 1
scsi
Clock0
Clock1
Trigger/sd0
Trigger/sd1
OUTPUT 2
scsi
Serial load0
Serial load1
reset0
reset1
test pulse0
test pulse1
Output
74xxx240
U12
U13
hcpl7100 x 6
U6
U7
U8
U9
U10
U11
U4 74F257
U5 74F257
+3V
+5V
-2V
0V
OE
jumper
J1
jumper
J2
jumper
J3
low
high
Pos Reg
LM317
2A FUSE
Neg Reg
LM337
KA337
-12V
-5.2V
VME
IDC
'100R'
U1 MC10125
U2 MC10125
U3 MC10125
clock
trigger
not reset
test pulse
Master Box
clock
load
reset
run/load
Pattern Gen
Serial data0
Serial data1
Decoupling detail
IC
+3V, +5V
0V
-2V, -5.2V
CLRC Rutherford Appleton Laboratory
ZEUS MVD Helix Driver Prototype
R. Halsall / J.Baker
4 Aug 98'



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