Test hybrid for the μvertex detector

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1 Introduction

This note describes the proposed layout of the hybrid circuit which will be used for the tests of the readout of the silicon planes of the ZEUS μvertex detector. As of today, the chip chosen for the front-end electronics is the HELIX 128S-2, developed for the HERA-B Silicon Vertex Detector and Inner Tracker at the ASIC laboratory of the University of Heidelberg. A detailed description of the chip functionality can be found in [1]. The layout presented here is intended to be used to develop and test the readout as well as to serve as a support for possible chip irradiation tests. In addition, it should allow the chips to be bonded to a detector or to arrays of input capacitors.
Following the discussions with U.Koetz and R.Carlin, a redundancy in the control and output lines, compared to the lines needed in the final version, was decided.
Apart from input signals, the HELIX chip features 136 bonding pads all around the four sides, used for the voltage supply, control and output signal. In the following sections, the electrical connections will be specified.
Since no consensus on the final design of the individual modules of the μvertex is yet achieved, the circuits will be built by layer deposition on an AlN substrate of ≈ 0.6 mm thickness, since this seems the most promising material at the moment. The hybrid masks design will be carried on by Mr. M.Sanchez of the ECP-PES division at CERN.

2 Overall layout

The requirements are the following:

- it is important to test the chips in daisy chain mode, where a token is exchanged between the chips to transfer the data on a common analog bus. The hybrid will be built to host 4 HELIX chips. This will not prevent the possibility to test one chip at a time: it should be feasible by bonding only one chip in the last position of the daisy chain.
- each HELIX chip integrates 128 channels. The spacing between the chips should be such that the circuit can be bonded, through a pitch adapter, to a detector of 120 μm pitch, as this will the readout pitch of the μvertex silicon planes.
- there will be no capacitors connected to the HELIX analog inputs directly on the hybrid. Input capacitors will be available on a service board. Therefore, the chips will be mounted flush to the edge of the hybrid, to allow to connect the board both to silicon planes and to a capacitor array.

- for the fan-out, a connector positioned at the edge of the hybrid opposite to the chips seems to be the most practical. Very small connectors (3.3 mm thick and 8 mm wide) are available at CERN and can be surface mounted on the hybrid[2].

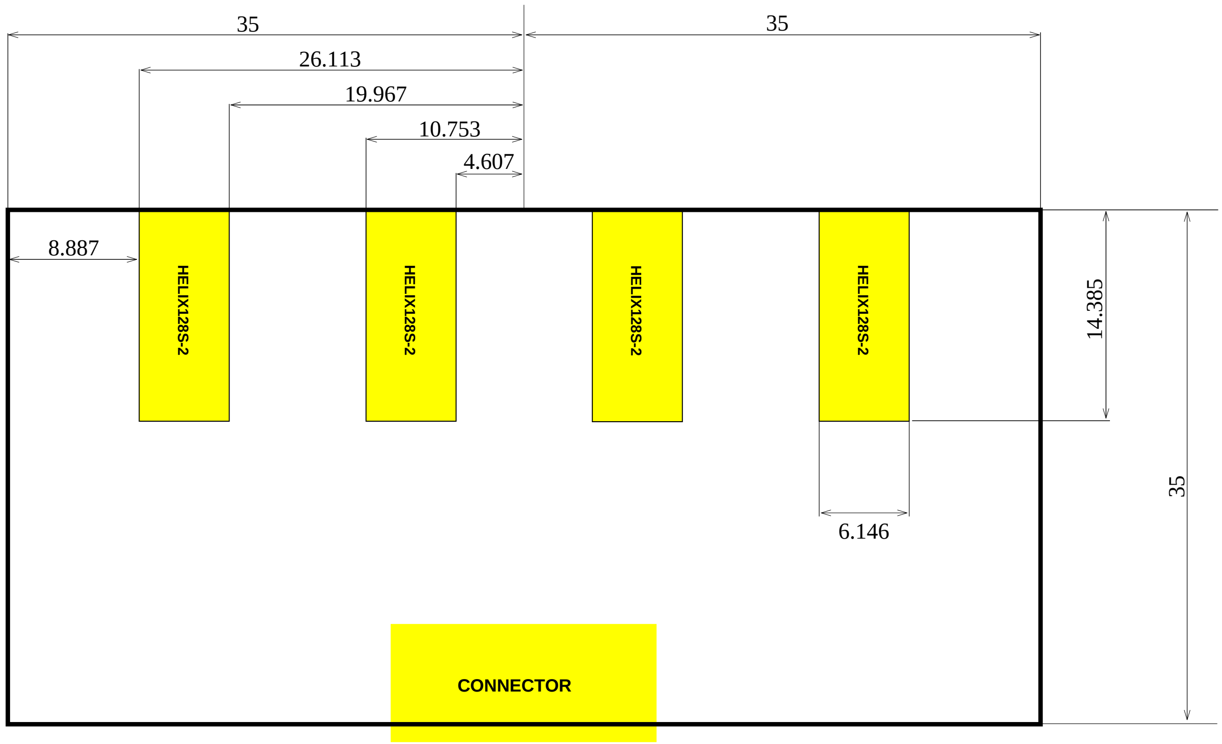

Figure 1: *Geometric layout of the hybrid showing the main components. Units are millimeters.*

The geometrical dimensions and positions of the main components are shown in fig. 1. The dimensions of the board are 70×35 mm^2, although the width can be increased by few millimeters if more space is needed.

3 Voltage and current supply

Two supply voltages (positive `Vdd` and negative `Vss`) plus a ground level (`Gnd`) are needed to operate the chip. The supply of the analog circuit, digital circuit and pad guard ring integrated in HELIX are independent and have to be connected separately to the voltage supply lines. In addition, the supply pads of the analog circuit are duplicated on all the sides of the chip to limit the voltage drop through the chip. Due to the desired position of the chips on the hybrid (see fig. 1) only the rear, bottom and top pads[1] can be connected. Finally, the chip base has to be at `Vss`, which defines its bulk potential.
The supply lines need to be as large as possible to limit the noise and the top layer should have a grid under each chip at `Vss` potential, so that each chip can glued on it using a conductive glue. As an example, the three layers of the hybrid designed for the HERA-B SVD

[1]Here "front side" refers to the side of the chip facing the detector, "rear" to the opposite side of the chip, "top" and "bottom" to the other two sides when the front side is on the left, as is the usual picture of the signal flowing from left to right.

Pad no.	HELIX pad name	Description	Connected to
133,134 263,264	**Gnda**	Analog grounds (0V)	**Gnd**
135,136 261,262	**Vssa**	Negative analog supply voltages (-2V)	**Vss**, need a filter capacitor (10 nF)
137,138 259,260	**Vdda**	Positive analog supply voltages (+2V)	**Vdd**, need a filter capacitor (10 nF)
238 237,236 235-232	**Vddg** **Vddd** **Vdda**	Positive supply voltages (+2V)	**Vdd**, need a filter capacitor (100 nF)
231-228 227,226 225	**Vssa** **Vssd** **Vssg**	Negative supply voltages (-2V)	**Vss**, need a filter capacitor (100 nF)
224	**Rref**	Internal Refrence current supply	**Vss** through 20 KΩ resistor
223	**IrefOut**	Internal reference current source	**IrefIn** (HELIX pad n0. 222) via a small bonding pad
222	**IrefIn**	Reference current input pad	**IrefOut** (HELIX pad n0. 223) via a small bonding pad
220	**Idriver**		a blocking capacitor (100 nF)
219	**Vdcl**		a blocking capacitor (100 nF)
218	**Vd**		a blocking capacitor (100 nF)

Table 1: *Connection of the HELIX pads to voltage and bias current supply on the hybrid circuit board.*

are shown in fig. 2.
One inductor plus a pair of capacitors should be used as filters both on `Vss` and `Vdd`. Smaller capacitors of $10 \div 100$ nF should also be added as close as possible to the input pads of the chip. Moreover, three HELIX pads (`Vd`, `Vdcl` and `Idriver`) need to be connected to external blocking capacitors. Finally, a reference current of 100 μA, generated internally by connecting the `Rref` HELIX pad to `Vss` through 20 KΩ resistor, must flow from the HELIX pads `IrefOut` to `IrefIn`. In order to connect the two pads, which are side-by-side on HELIX, a small bonding area facing the pads must be available on the hybrid.

The circuit for the voltage and current supply is shown in fig. 3. A bias voltage line `vBias` for detector facing the chips has been added; a corresponding bonding area should be available in the upper right corner of fig. 1 and should extend as much as possible along the upper edge of the hybrid. The list of HELIX pads used and their connections is summarized in tab. 1. For the pad positions on the HELIX chip, please refer to fig.6.

4 Digital control signals and serial data load

Nine digital control signals and serial data for downloading the HELIX registers should be distributed in parallel to all the chips on the hybrid. In order to avoid any noise on the chip, the clock lines on the hybrid (`sclk`, `rclk` and `serClk`) and the trigger input line (`trig`) should be surrounded by grounded lines. Each chip can also be given an address by connecting the `Id`$\langle n \rangle$ HELIX pads to `Vdd` according to the specified address bit pattern. The list of pads

Pad no.	HELIX pad name	Description	Connected to
177	`TransmitEnable`	Enables data transmission	`tEnab` line
198	`Sclk`	Sampling clock	`sclk` line
199	`Rclk`	Readout clock	`rclk` line
200	`Serclk`	Clock for serial data load	`serClk` line
201	`TrigIn`	Trigger input signal	`trig` line
202	`SerData`	Serial data	`sData` line
203	`SerLoad`	Load signal for serial line	`load` line
206	`notReset`	Reset signal	`notReset` line
208	`FcsTp`	Test pulse signal	`fcsTp` line
214 ⋮ 209	`Id`⟨0⟩ ⋮ `Id`⟨5⟩	Chip address	positive voltage `Vdd` according to the desired chip address.

Table 2: *Connection of the HELIX pads to digital control lines on the circuit.*

used and their connections to the different lines is summarized in tab. 2. The corresponding circuit diagram is shown in fig. 4.

5 Daisy chain

In daisy chain mode, a token to syncronize the data output is exchanged between the chips through the `HelixTokenIn/Out` and `ReturnTokenOut/In` HELIX pads. In addition, the syncronicity is monitored with the `SyncIn/Out`$\langle n \rangle$ pads and errors are collected by the last[2] chip in the chain. The connections are only between neighbouring chips; the only exception is `SyncOut`$\langle 5 \rangle$ of the last chip of the chain, which should be used as output `DataValid` signal (see next paragraph). The list of pads used and their connections is summarized in tab. 3.

6 Output signals

The *analog* output signals of each chip are `AnalogOut` and `AnalogOutDummy`. They are read out on a common output bus, `aout` and `notAout` respectively. In addition, each HELIX has a test preamplifier output (`TestOut` which we want to read separately for each chip through the lines `test1` $\cdots$ `test4`.
The *digital* output signals are `DataValid` and `Error` and are collected through the `dValid` and `error` lines. In *daisy chain mode*, both signals should be collected from the last chip in the chain and the or of the `DataValid` of each HELIX in the chain is available as `SyncOut`$\langle 5 \rangle$.
In *standalone* mode (i.e. the hybrid is used to run only one HELIX), the chip should be glued in the rightmost slot of fig. 1. Here, the `DataValid` signal should be collected from the `DataValid` HELIX pad. Finally, a `FifoFull` signal should be read separately for each chip (`fFull1` $\cdots$ `fFull4`).

The list of output pads used and their connections is summarized in tab. 4. The correspoding circuit can be found in fig 5.

[2]The token exchange proceeds from left to right in fig. 1; "first" and "last" chips in the chain are respectively the leftmost and rightmost in that picture.

Pad no.	HELIX pad name	Description	Connected to
179	`HelixTokenIn`	Input token	`HelixTokenOut` (HELIX pad no. 257) of the preceding chip in the chain. Not connected in the first chip of the chain.
180	`ReturnTokenOut`	Output return token	`ReturnTokenIn` (HELIX pad no. 256) of the preceding chip in the chain. Not connected in the first chip of the chain.
181	`SyncIn`⟨0⟩	Syncronicity monitor input	`SyncOut`⟨0⟩ (HELIX pad no. 255) of the preceding chip in the chain. Not connected in the first chip of the chain.
182	`SyncIn`⟨1⟩	Syncronicity monitor input	`SyncOut`⟨1⟩ (HELIX pad no. 254) of the preceding chip in the chain. Not connected in the first chip of the chain.
183-185	⋮	⋮	⋮
182	`SyncIn`⟨5⟩	Syncronicity monitor input	“ “
257	`HelixTokenOut`	Output token	`HelixTokenIn` (HELIX pad no. 179) of the following chip in the chain. Not connected in the last chip of the chain.
256	`ReturnTokenIn`	Input return token	`ReturnTokenOut` (HELIX pad no. 180) of the following chip in the chain. Not connected in the last chip of the chain.
255	`SyncOut`⟨0⟩	Syncronicity monitor output	`SyncIn`⟨0⟩ (HELIX pad no. 181) of the following chip in the chain. Not connected in the last chip of the chain.
254	`SyncOut`⟨1⟩	Syncronicity monitor output	`SyncIn`⟨1⟩ (HELIX pad no. 182) of the following chip in the chain. Not connected in the last chip of the chain.
253-251	⋮	⋮	⋮
250	`SyncOut`⟨5⟩	Syncronicity monitor output	`SyncIn`⟨5⟩ (HELIX pad no. 186) of the following chip in the chain. See also tab. 4

Table 3: *Connection of the HELIX pads for daisy chain operation.*

Pad no.	HELIX pad name	Description	Connected to
178	`FifoFull`	Readout fifo overflow	`fFull1`···`fFull4` lines
204	`Error`	Error condition in a chip	`error` line, *only for the last chip of the chain.*
205	`DataValid`	valid data on analog output line `aout` and `notAout`	`dValid` line (standalone mode). *Only for rightmost chip.*
215	`AnalogOut`	serial analog output	`aout` line
216	`AnalogOutDummy`	dummy serial analog output	`notAout` line
250	`SyncOut`⟨5⟩	Syncronicity monitor output	`dValid` line (daisy chain mode). *Only in the last chip of the chain.*
258	`TestOut`	Test preamplifier output	`test1`···`test4` lines

Table 4: *Connection of the output HELIX pads on the hybrid circuit lines.*

Name	Description	Connection to HELIX pads
`Gnd`	Ground	`Gnda`
`Vss`	Negative supply voltage	`Vssa, Vssd, Vssg`
`Vdd`	Positive supply voltage	`Vdda, Vddd, Vddg`
`vBias`	Bias voltage for detector	none
`tEnab`	Enable data transmission	`TransmitEnable`
`sclk`	Sampling clock	`Sclk`
`rclk`	Readout clock	`Rclk`
`serClk`	Serial data clock	`Serclk`
`trig`	Trigger input	`TrigIn`
`sData`	Serial data input	`SerData`
`load`	Load serial data	`SerLoad`
`notReset`	Reset signal	`notReset`
`fcsTp`	Test pulse	`FcsTp`
`aout`	Analog output	`AnalogOut`
`notAout`	Dummy analog output	`AnalogOutDummy`
`dValid`	Analog output valid	`AnalogOut` of HELIX no. 4 `SyncOut`⟨5⟩ of HELIX no. 4
`error`	Error during readout	`Error` of HELIX no. 4
`fFull1`	Readout fifo overflow in HELIX no.1	`FifoFull` of HELIX no. 1
`fFull2`	Readout fifo overflow in HELIX no.2	`FifoFull` of HELIX no. 2
`fFull3`	Readout fifo overflow in HELIX no.3	`FifoFull` of HELIX no. 3
`fFull4`	Readout fifo overflow in HELIX no.4	`FifoFull` of HELIX no. 4
`test1`	Test preamplifier output of HELIX no.1	`TestOut` of HELIX no. 1
`test2`	Test preamplifier output of HELIX no.2	`TestOut` of HELIX no. 2
`test3`	Test preamplifier output of HELIX no.3	`TestOut` of HELIX no. 3
`test4`	Test preamplifier output of HELIX no.4	`TestOut` of HELIX no. 4

Table 5: *List of all the lines on the hybrid circuit board. The HELIX chip numbering goes from the leftmost to the rightmost in fig. 1.*

7 Conclusion

The list of the input/output signals of the hybrid is summarized in tab. 5 together with the connection to the HELIX chip pads. A drawing of HELIX128S-2 showing the pads location has also been added in fig. 6.

References

[1] M.Feuerstack-Raible, B.Glass, W.Fallot-Burghardt, U.Trunk, *Helix128S-2 User Manual Version 1.3* HD-ASIC-33-0697.
`http://www.ihep.uni-heidelberg.de/Asic/HeraB/Helix128S2_html/helix.html`

[2] M.Sanchez, private communication.

[3] These pictures were kindly provided by Mr. Christian Bauer.

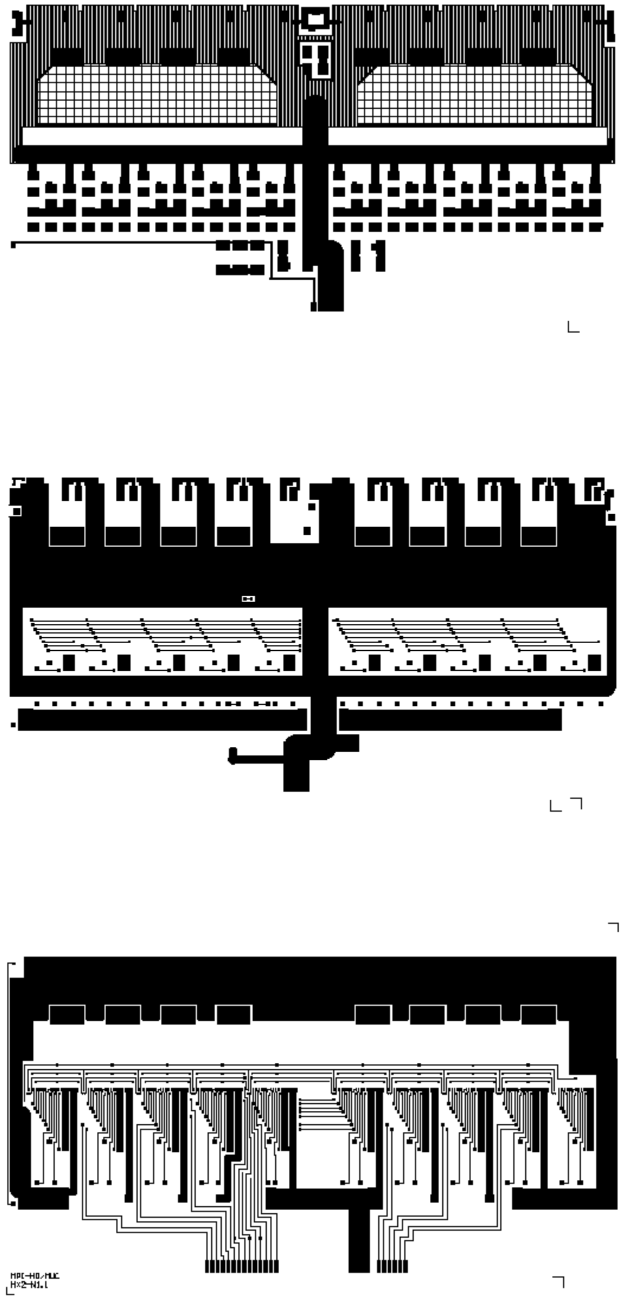

Figure 2: *Masks of the three gold layers, top, middle and lower (from above to below), of the the HERA-B SVD hybrid [3]. The very large lines are at* Vss *potential (top), at ground (middle) ad at* Vgg *potential (lower). The grid on the top layer is needed to define the bulk potential of the HELIX chip.*

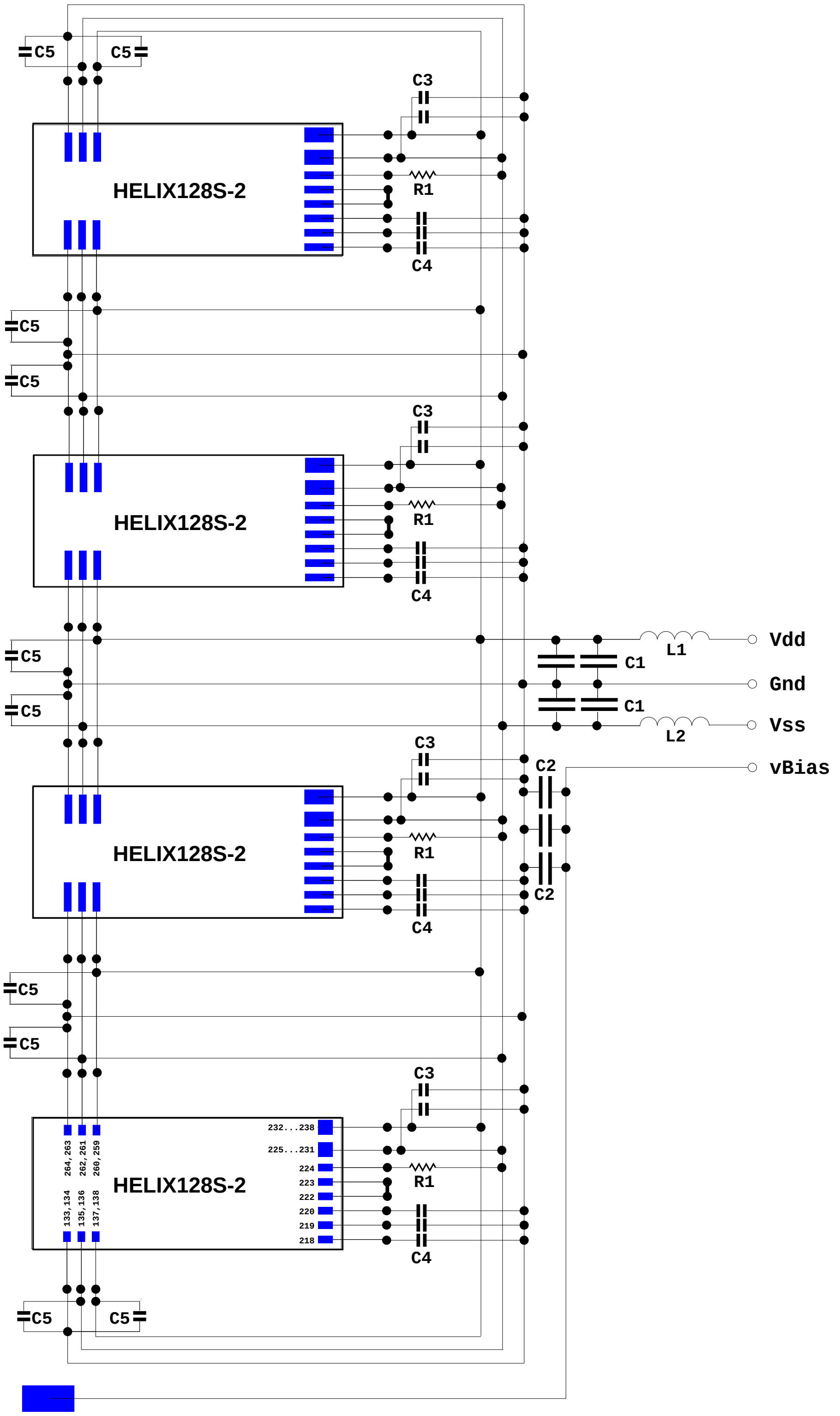

Figure 3: *Circuit diagram for the voltage supply of the HELIX chips. Inputs are* `Vdd` *(+2V),* `Vss` *(-2V) and* `Gnd` *(ground). In addition, a line needed to bring the bias voltage to the detector (*`vBias`*) has been added. The components shown have the following values:* `C1`$= 4.7\mu F$*,* `C2`$= 220nF$*,* `C3`$=$`C4`$= 100nF$*,* `C5`$= 10nF$*,* `R1`$= 20k\Omega$*. For the HELIX pad positions and numbers please refer to fig. 6 and tab. 1.*

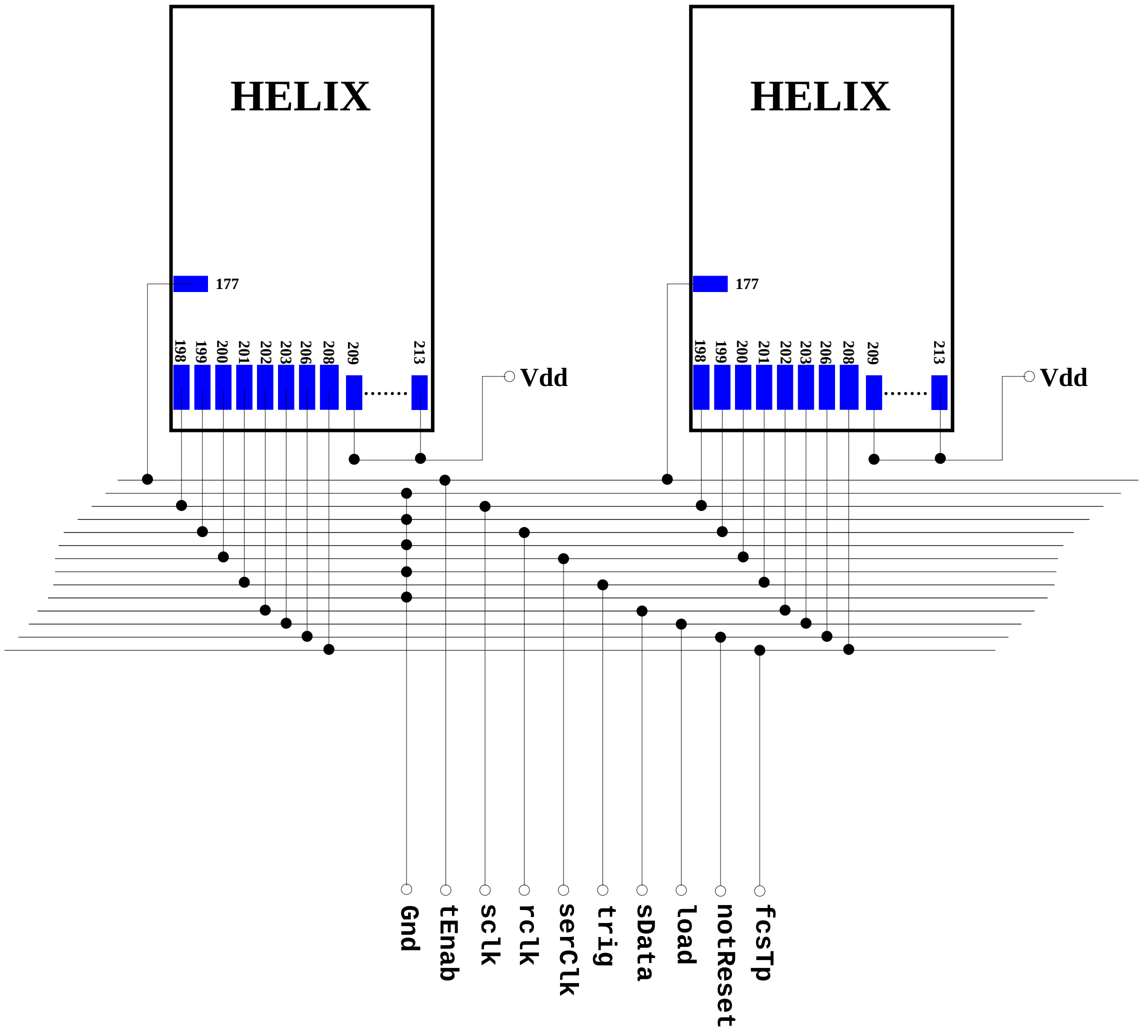

Figure 4: *Circuit diagram for the digital control of the HELIX chip (only two chips have been shown in the picture). The three clock lines (*`sclk`*,* `rclk` *and* `serClk`*) and the trigger input line (*`trig`*) are surrounded by ground lines. The pads* $209\cdots214$ *are the chip address and should be connected to* `Vdd` *according to the desired chip address bit pattern. For the pad description and position, refer to tab. 2 and fig. 6*

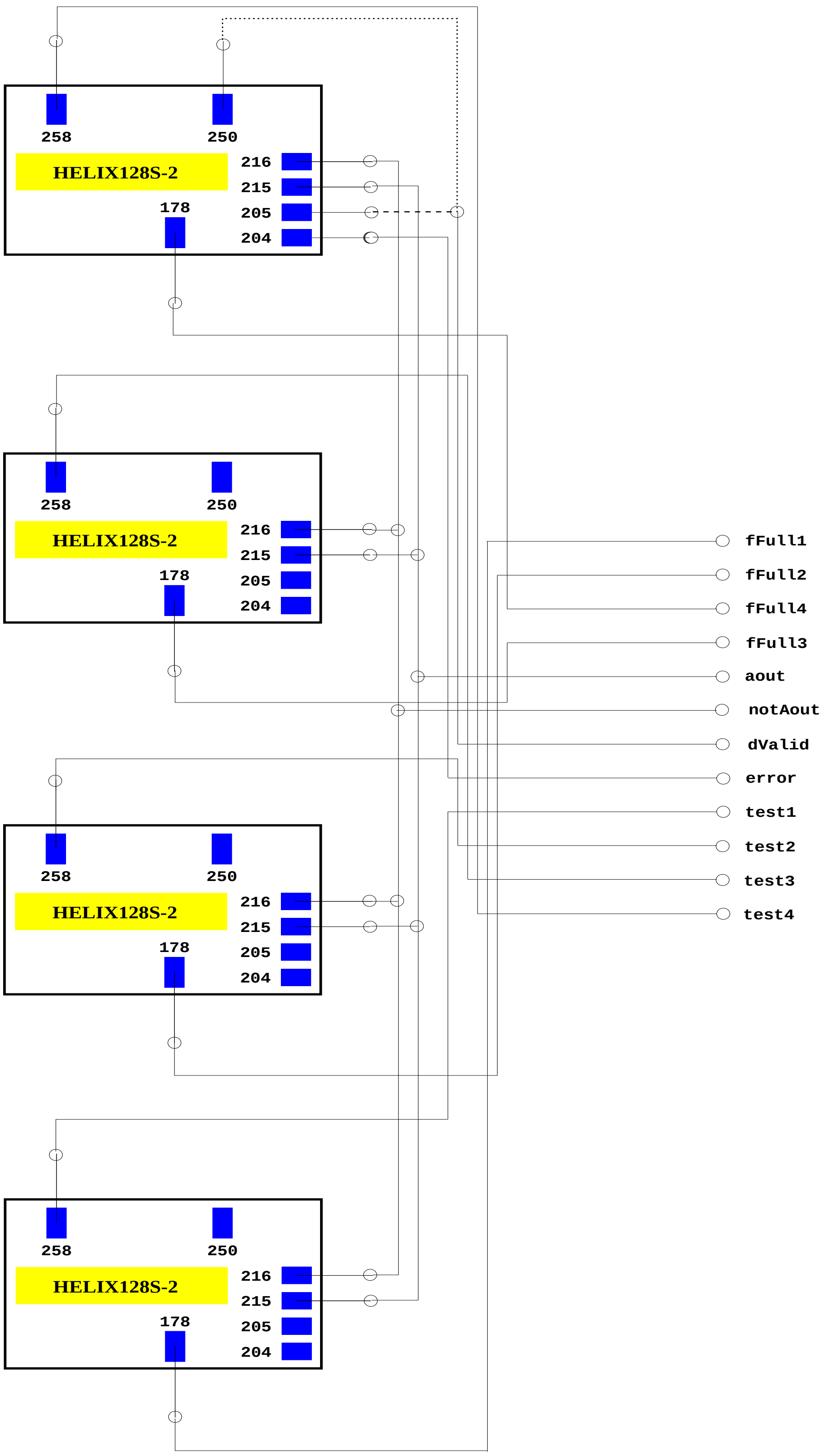

Figure 5: *Circuit diagram of the different output signals of the HELIX chips. The dashed line indicates the connection for running HELIX in standalone mode. The dotted line indicates the connection for running HELIX in daisy chain mode. For the HELIX pad description and position, refer to tab. 4 and fig. 6*

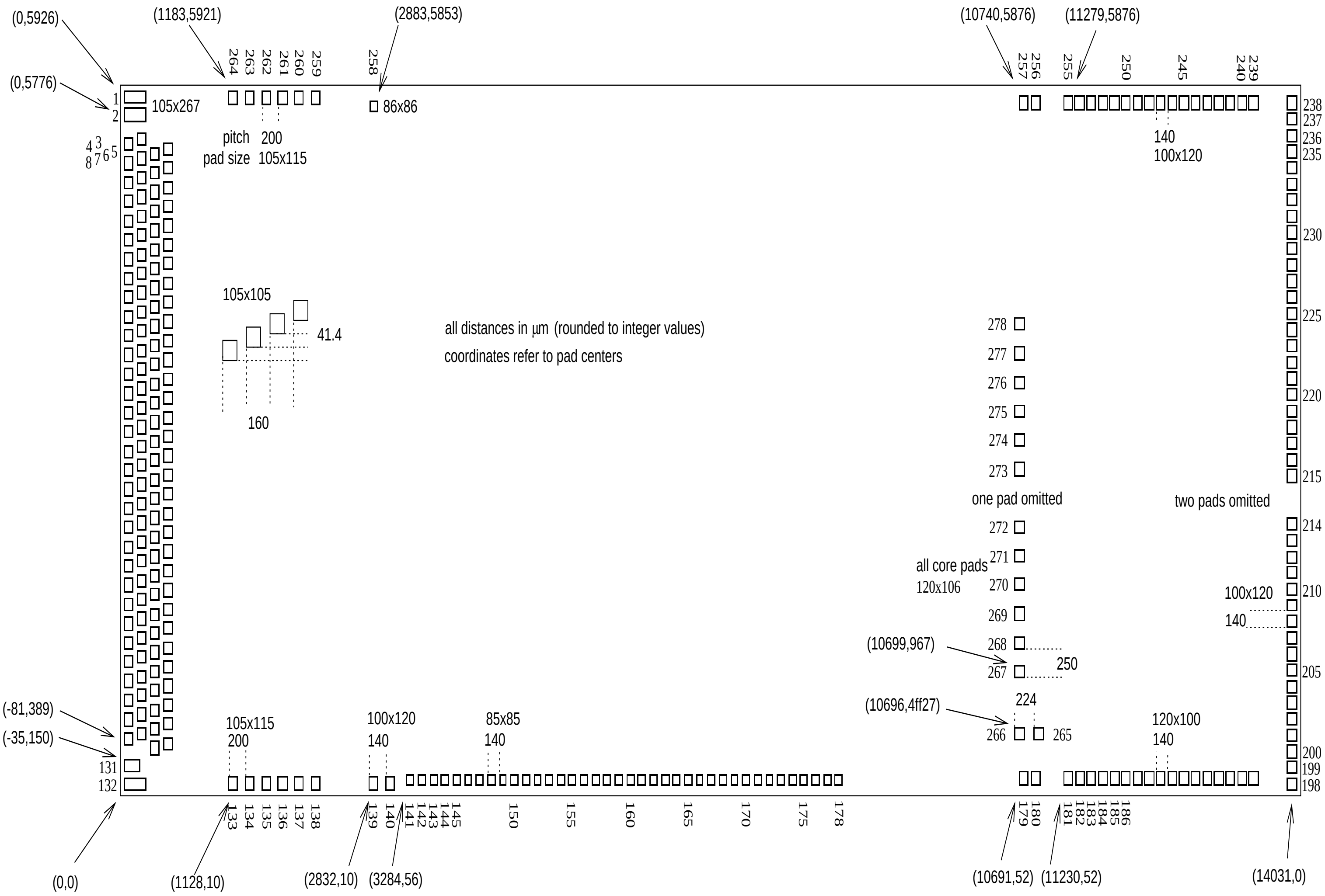

Figure 6: *Schematic drawing of HELIX128S-2 taken from [1], showing the pad locations. The overall chip dimension is* $14.385 \times 6.146\ mm^2$.