

## **Project Specification**

**Project Name: ZEUS MVD HELIX Interface**

**Version:** feasibility study draft

**Approval:**

	<b>name</b>	<b>signature</b>	<b>date</b>
<b>Project Manager</b>	<b>XXXXXXXXXX</b>	<b>XXXXXXXXXX</b>	<b>9 March 98</b>

**Distribution for all updates:**

**Project Manager:**

**Customer:** Jon Butterworth, Val Noyes

**Group Leader responsible for Project:** Rob Halsall

**Project Managers of related projects:**

**Additional distribution at PDR and FDR:** John Lane

**System Design Group Leader:** R. Halsall

**Micro Electronics Design Group Leader:** M. French

**Design Support Group Leader:** S.P.H. Quinton

**Management Support Services Group Leader:** Chris Lowe

**Electrical Systems Design Group Leader:** J.F. Connolly

## 1.0 Scope

ZEUS Microvertex Detector (ZEUS MVD) upgrade. Helix Interface consists of HELIX Fanout module & HELIX Driver module.

## 2.0 Related projects and documents

ZEUS MVD, ZEUS MVD Masterbox, HELIX Front End, ADC & ZEUS Slow Control DAQ.

DAQ Document

[http://www-zeus.desy.de/~polini/ZEUS\\_ONLY/mvdda/mvdda.html](http://www-zeus.desy.de/~polini/ZEUS_ONLY/mvdda/mvdda.html)

Helix documentation

Masterbox documentation

ADC documentation

## 3.0 Technical Aspects

Refer to external document

### 3.1 Requirements

Masterbox to MVD HELIX Front End clock & fast control fanout

VME to MVD HELIX FE configuration setup fanout

system setup down load time < 1 second

serial channels independent

Additional Modes, Stand alone Self test?

Additionally Front End power fail safe protection

Additionally special shifted CMOS/LVDS signal levels for +/-2V HELIX FE ?

### 3.2 Specification of deliverables

6U VME Module, Single Width

VME; Minimum 32 Bit slave interface

Input; differential ecl, clock, trigger, test pulse & not reset, 2 pin lemo00

Output; 16 x (differential: clock, trigger/serial data in, single ended test pulse, not reset, serial load) 64 Differential, 48 co-ax, Target 16 output sets

Timing; to be determined

Connectors & Cables; STP, co-ax, 2 pin + shield lemo00, amplimite

Control Registers; Test Pulse mask Register, general Status Register, general Control Register, download register(s), Trigger

Memory; 16 x 8 HELIX x 20 bits x 17 registers  
16 x 8 x 4 x 32 = 16K Bytes

Block Diagram;



Project Manager/Engineer Greg Johnson/Trevor Slade  
Project Consultants Rob Halsall/Adam Baird  
Test Engineer ?

## **4.2 Deliverables**

HELIX Driver Prototypes 1 required, 1-3 Spares ?  
HELIX Driver Production 16 in system + spares

HELIX Fanout 1-2 in system?

Customer Supplied; Software, Crate, Processor

Motorola Power-PC VME board computer (MVME2600) /Lynx-OS

## **4.3 Project plan**

Hekix Driver Prototype

Project Spec March		
Preliminary Design Review		
Design 1	schem layout	April-May
Intermediate Design Review		
Design 2	pcb tapeout	June 1
Manufacture		June 2-4
Assembly		July 1
Test		July 2-4
Ready		start of August
HELIX Driver Production;		
Installed & Commissioned		Q3 99
Helix Fanout Prototype;		
Installed & Commissioned		Q1 99
Helix Fanout Production		
Installed & Commissioned;		Q3 99
Refer to Project Plan Gantt Chart		

## **4.4 Design Reviews**

Customer & Engineers will attend Intermediate & Final Design Reviews

## **4.5 Training**

RH Define

## **4.6 CAE and test equipment**

RH Define

#### **4.7 Costs and finance**

Estimated Effort (Staff Months);

Engineer	4+1
OM	0.5
DO	1
Test	1

Total Effort 6-9 months

Estimated Component Costs;

£1-2K Module

Travel;

RAL, UCL, DESY, Video Conf

Cost Centres;

Effort	FC76000		QXXXX	
Travel	FC77400	TDD	QXXXX	TDD
Components	FC76400	TDD	QXXXX	TDD

#### **4.8 IPR and confidentiality**

Not confidential, CCLRC owns IPR

#### **4.9 Safety**

Signal/HELIX FE power supply fail safe - Safety Critical for HELIX chip

DISCLAIMER

#### **4.10 Environmental impact**

Standard terms