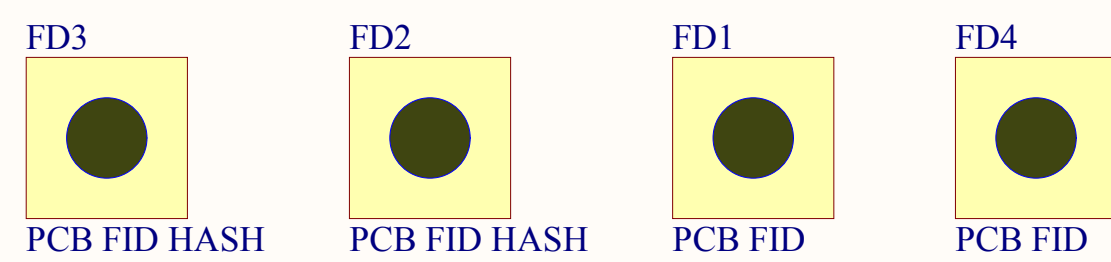
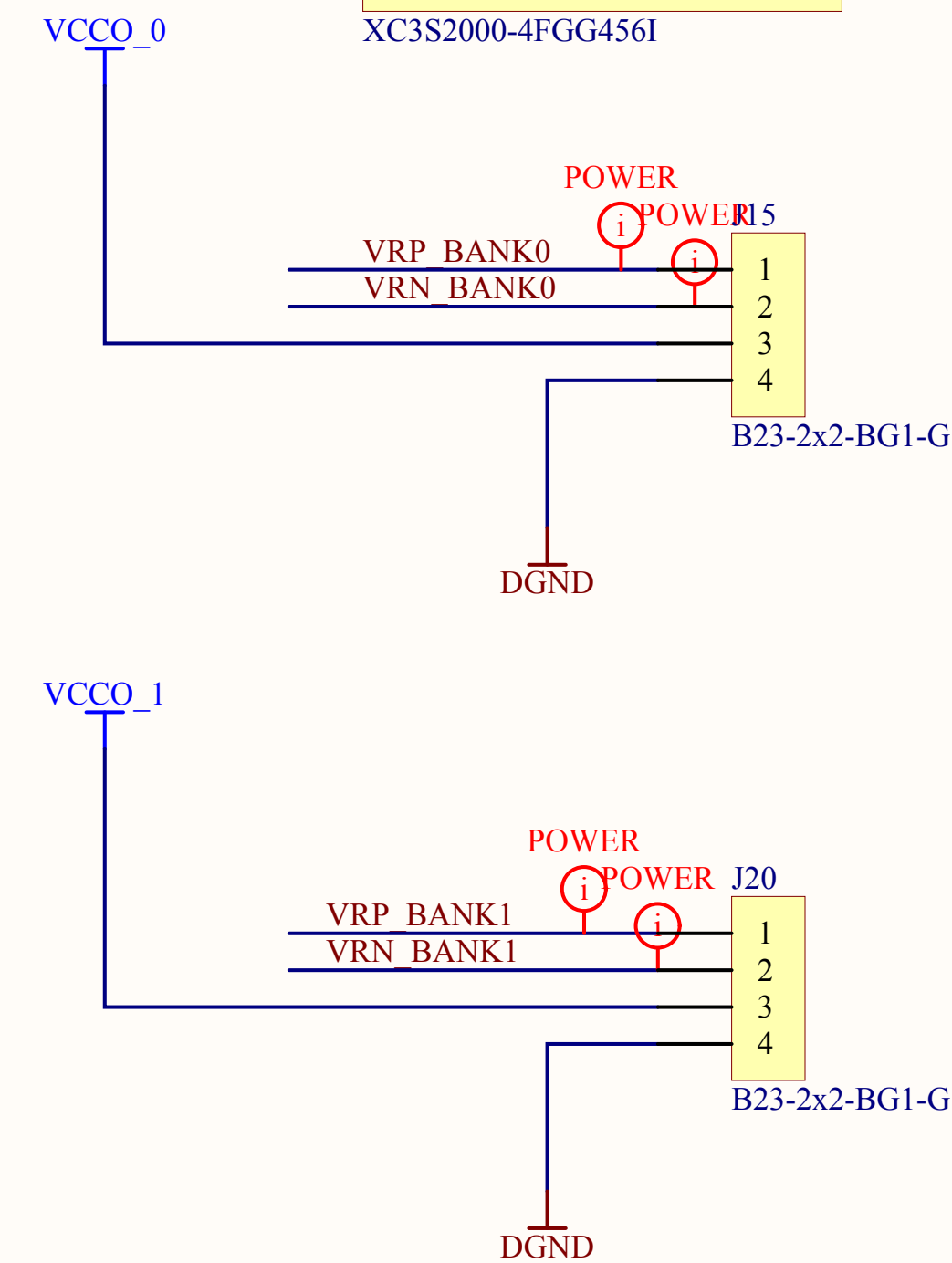
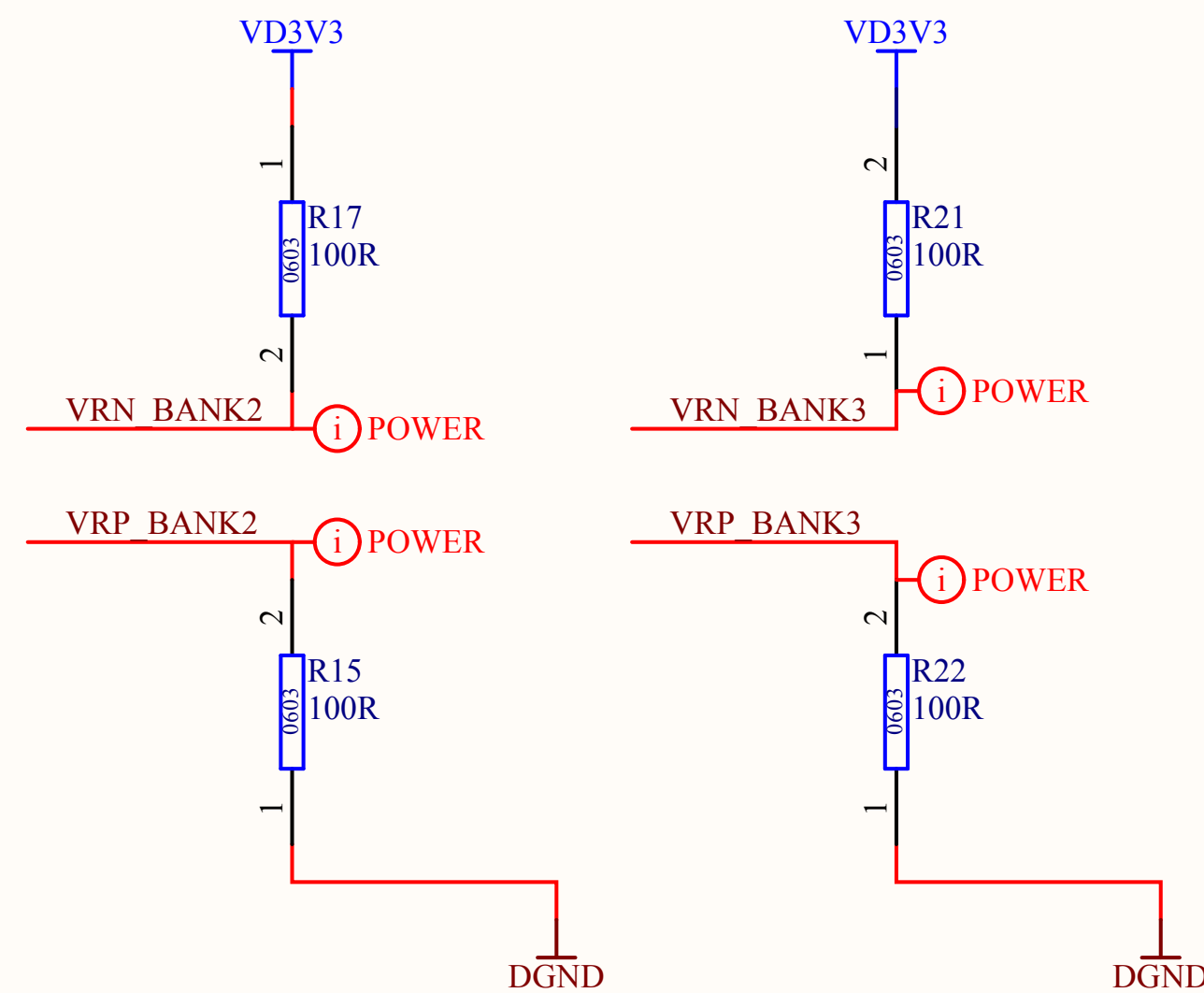
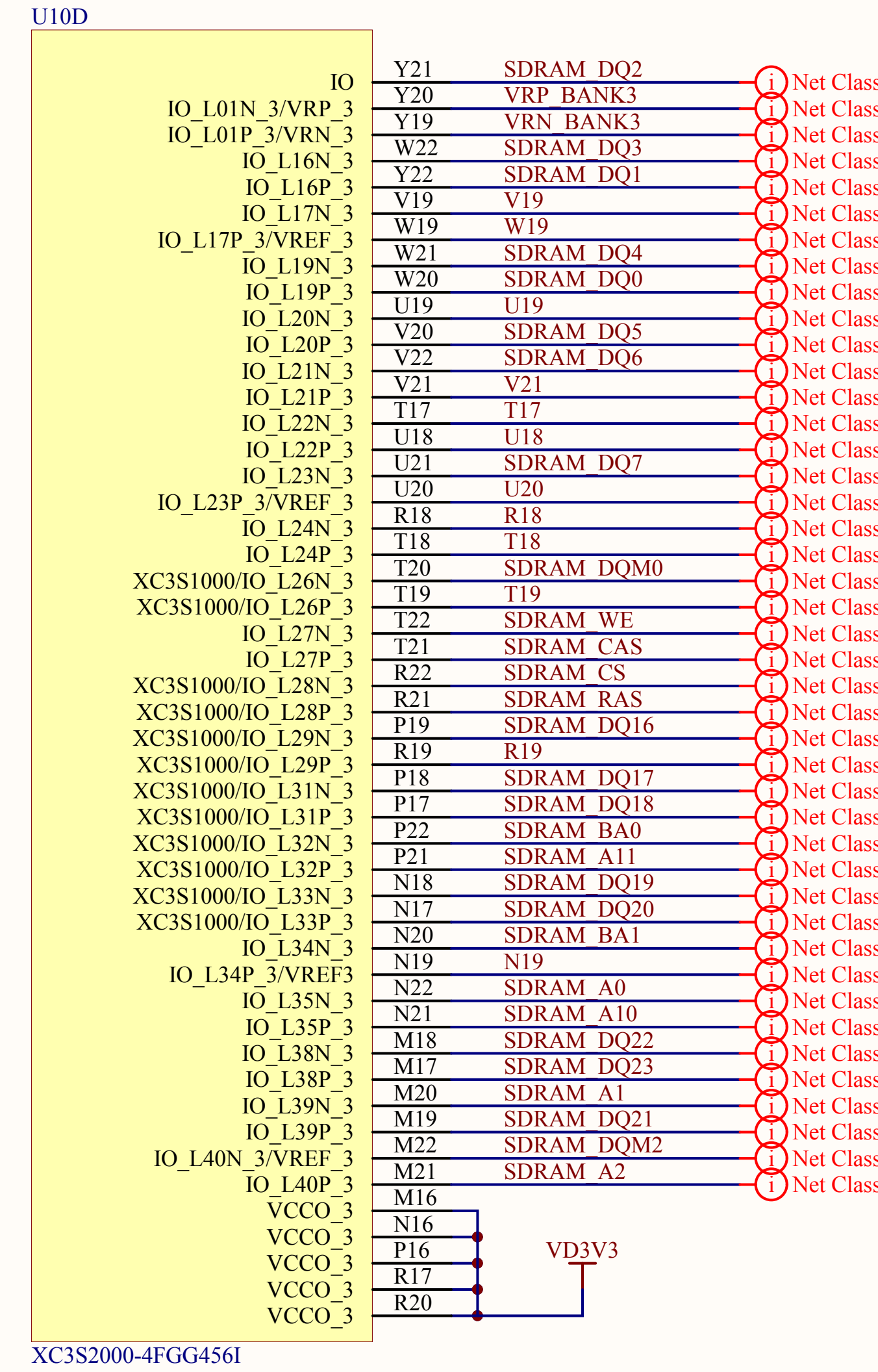
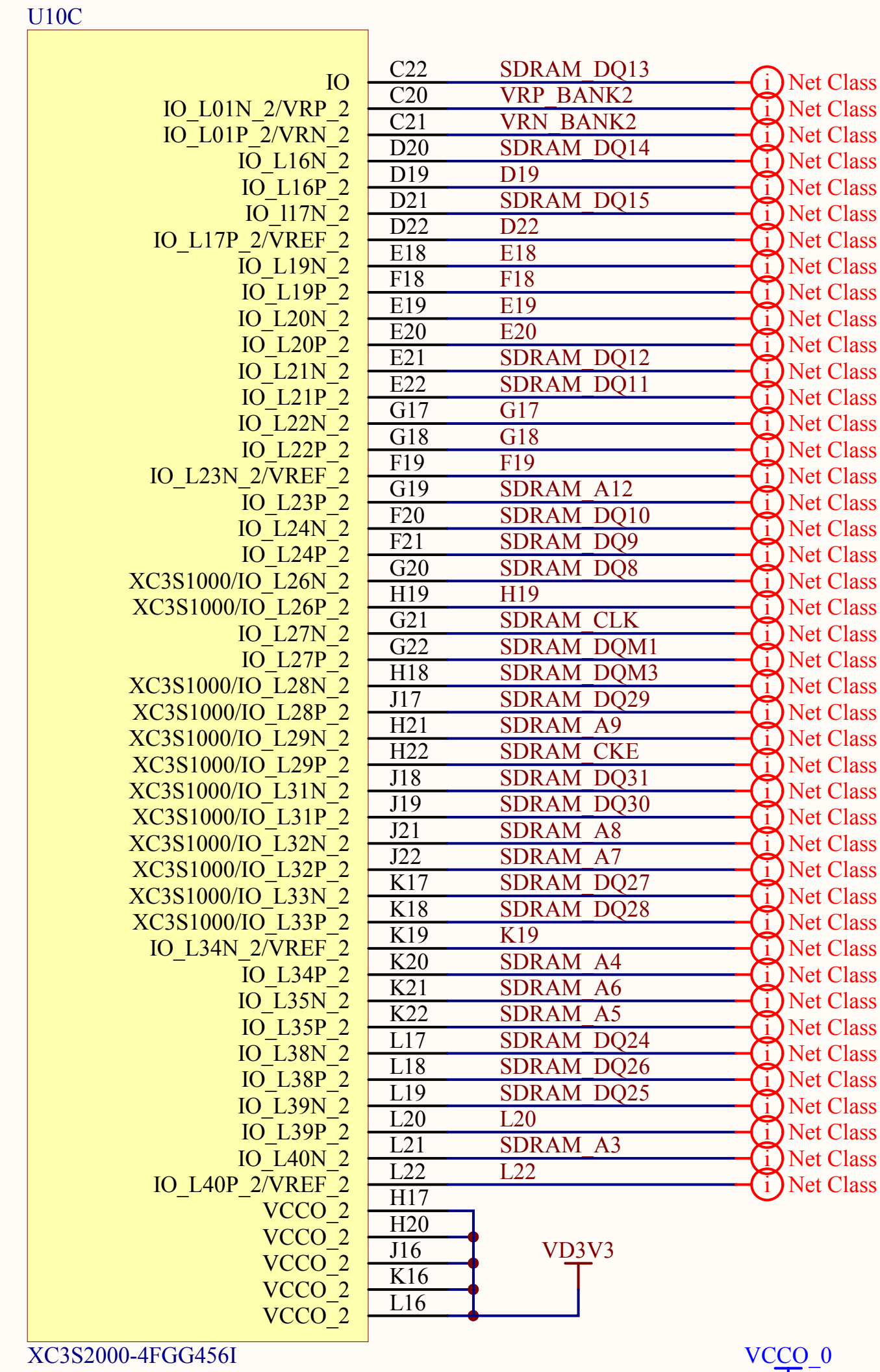
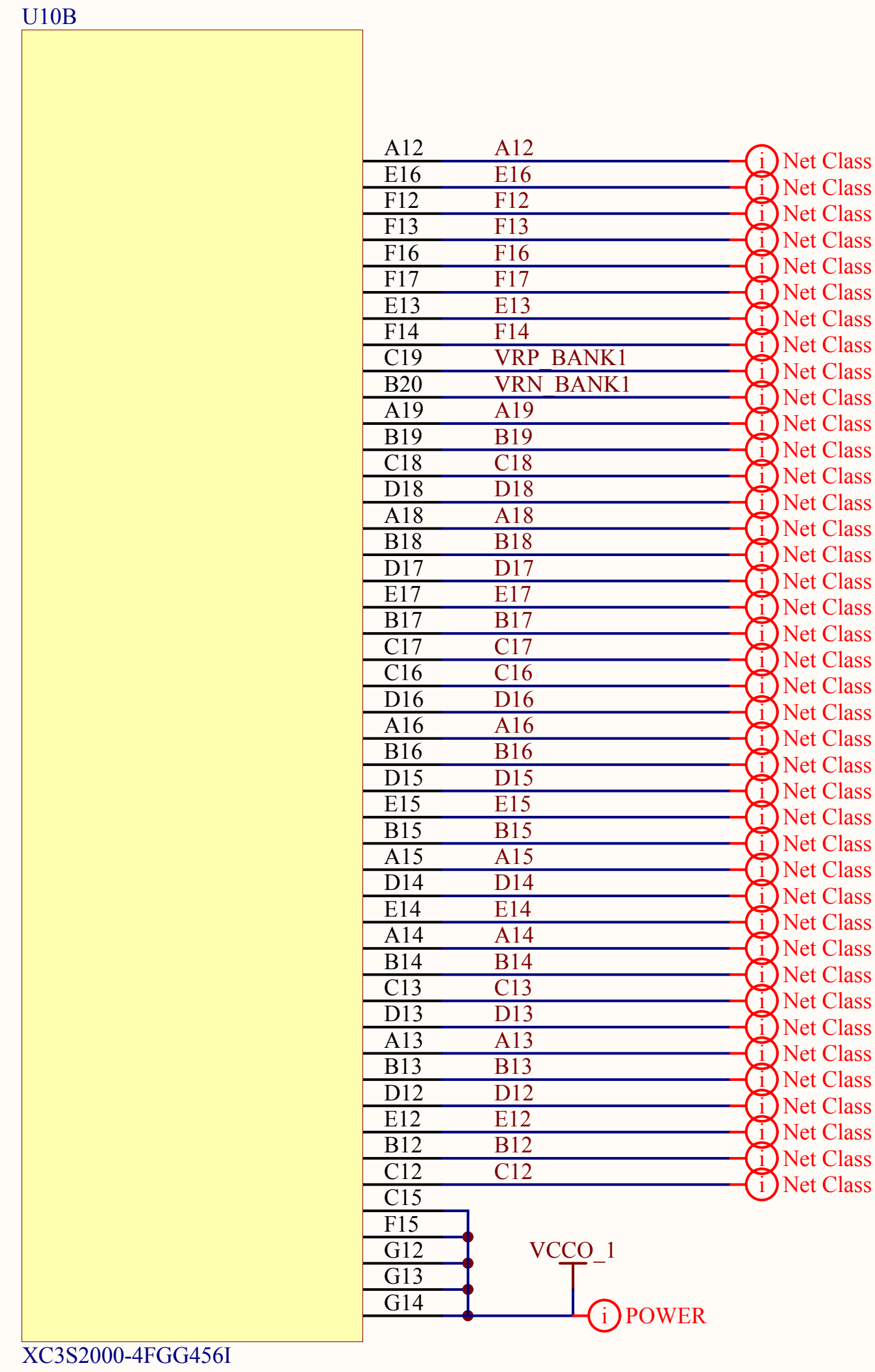
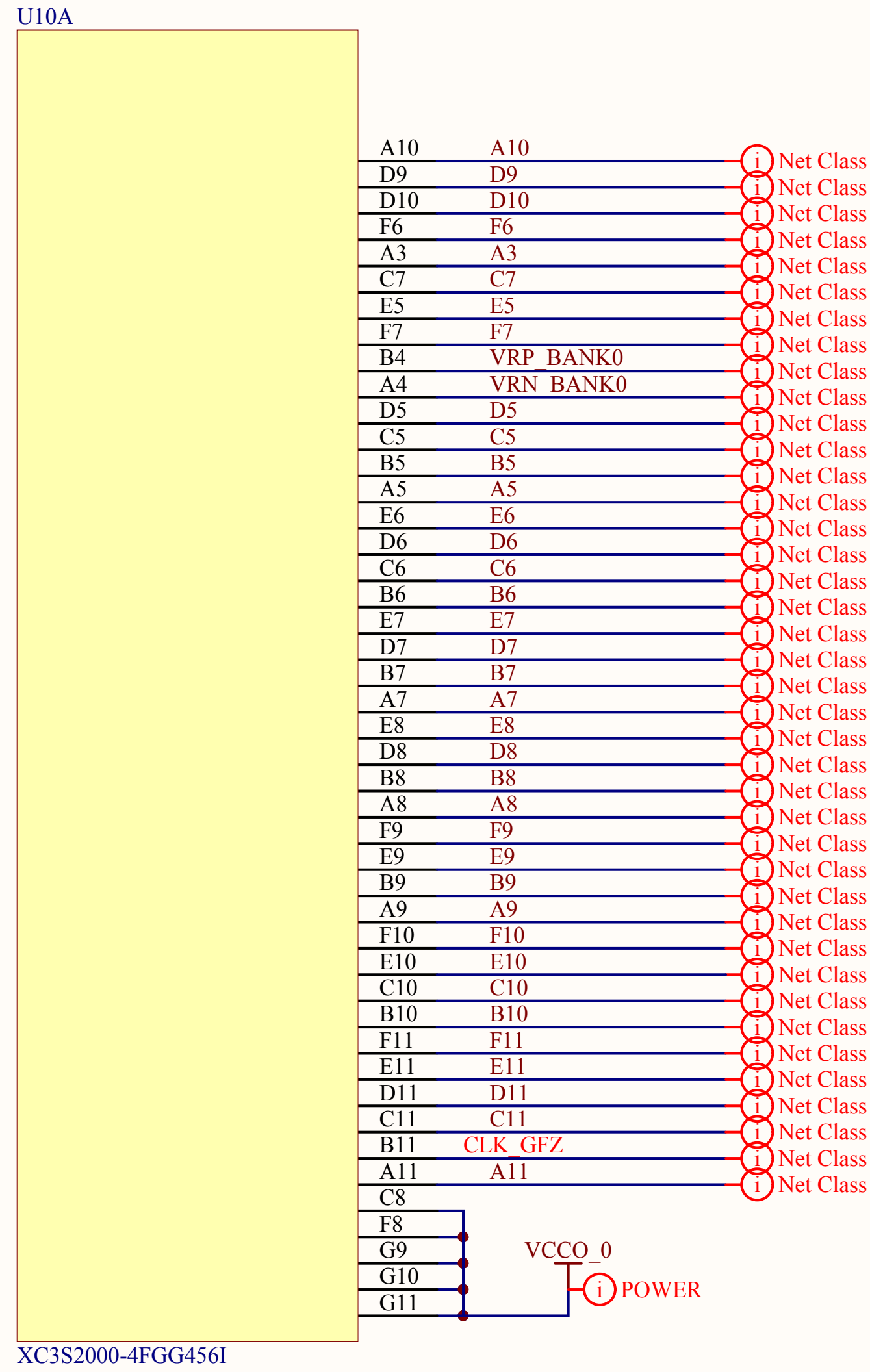
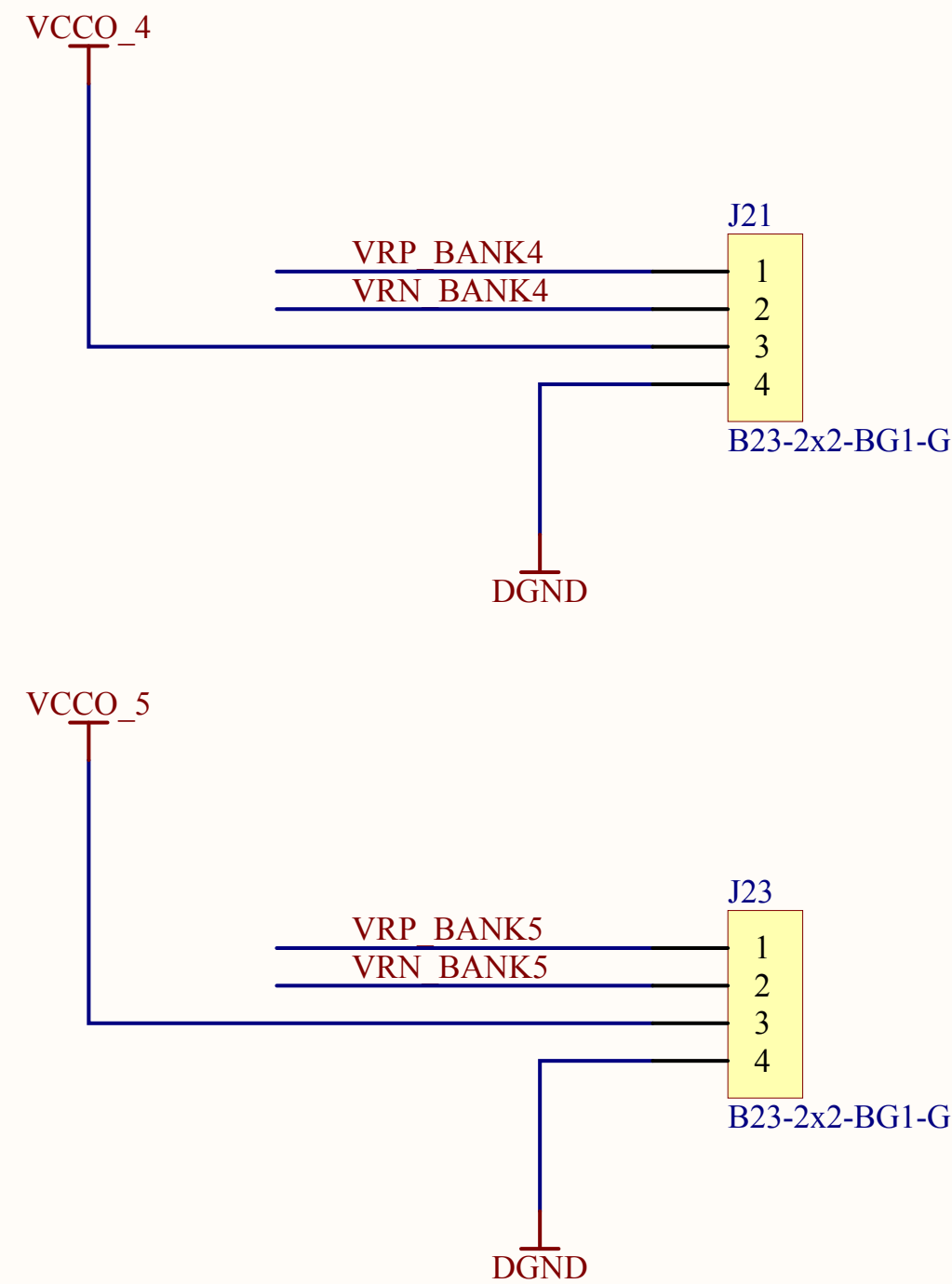
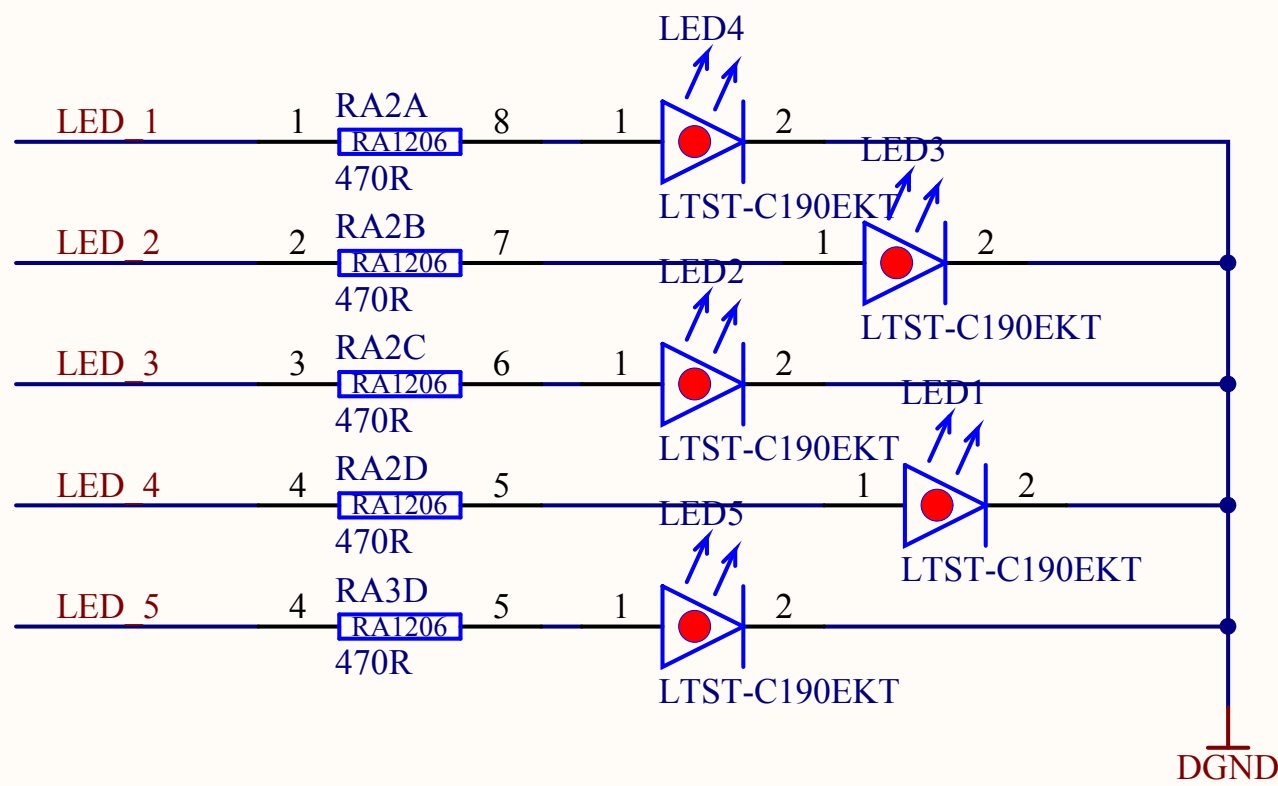
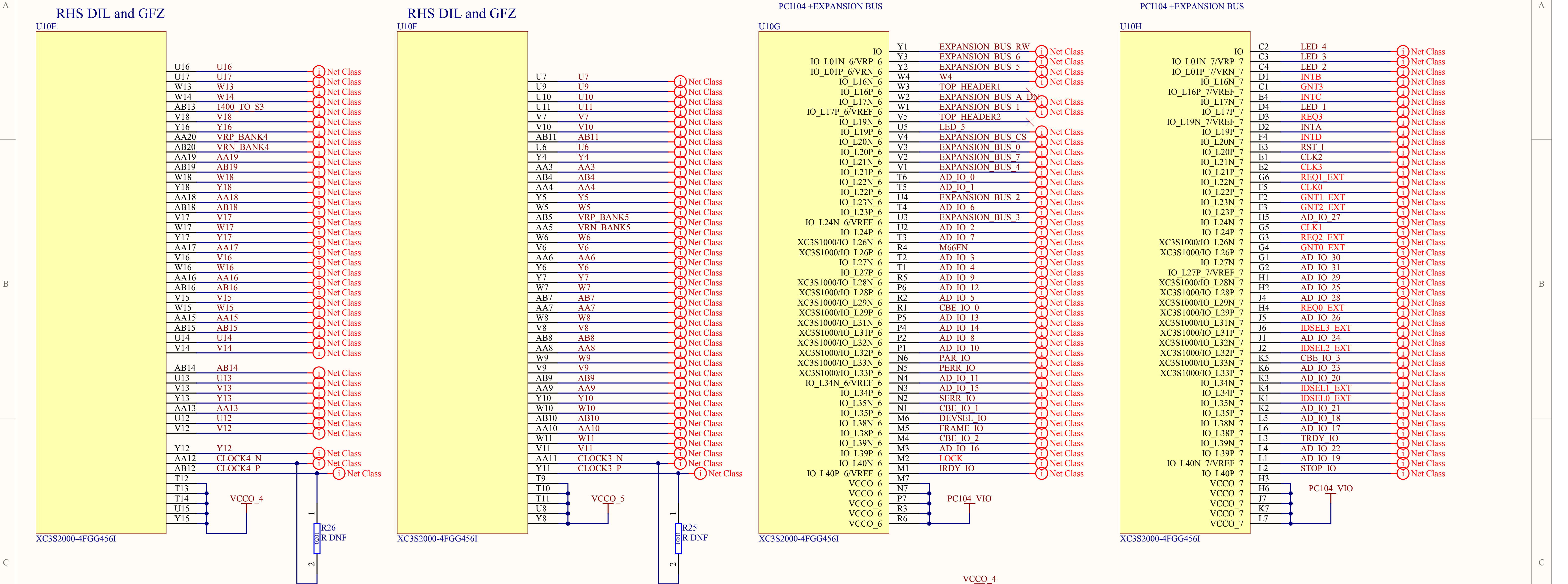


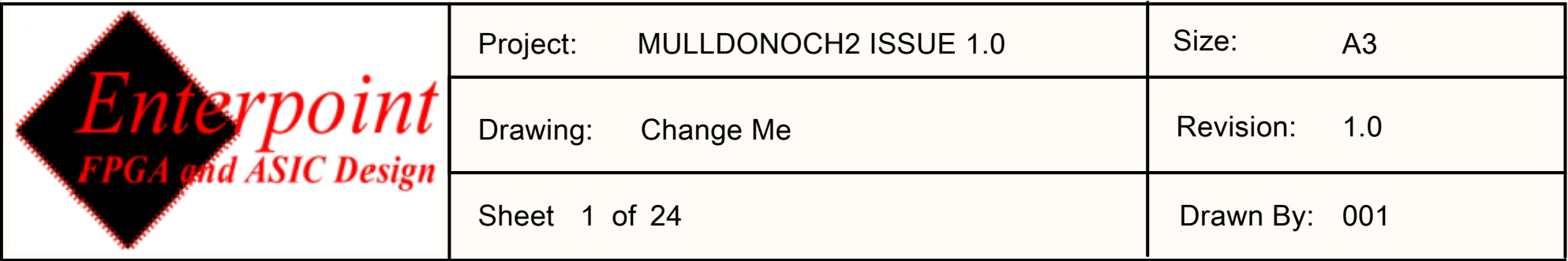
LHS DIL and GFZ

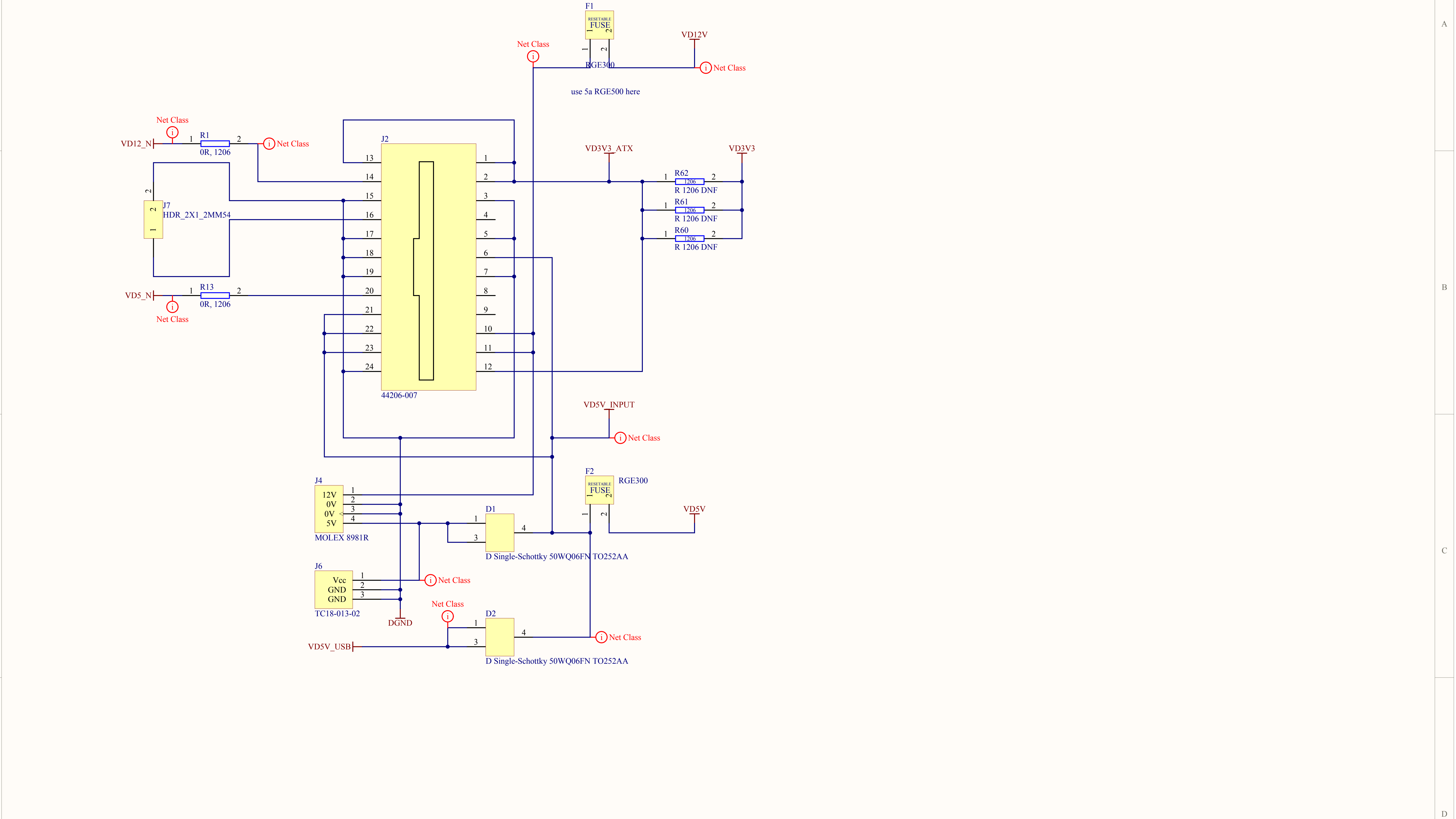
E5 IS SPARE GOING NOWHERE


LHS DIL and GFZ









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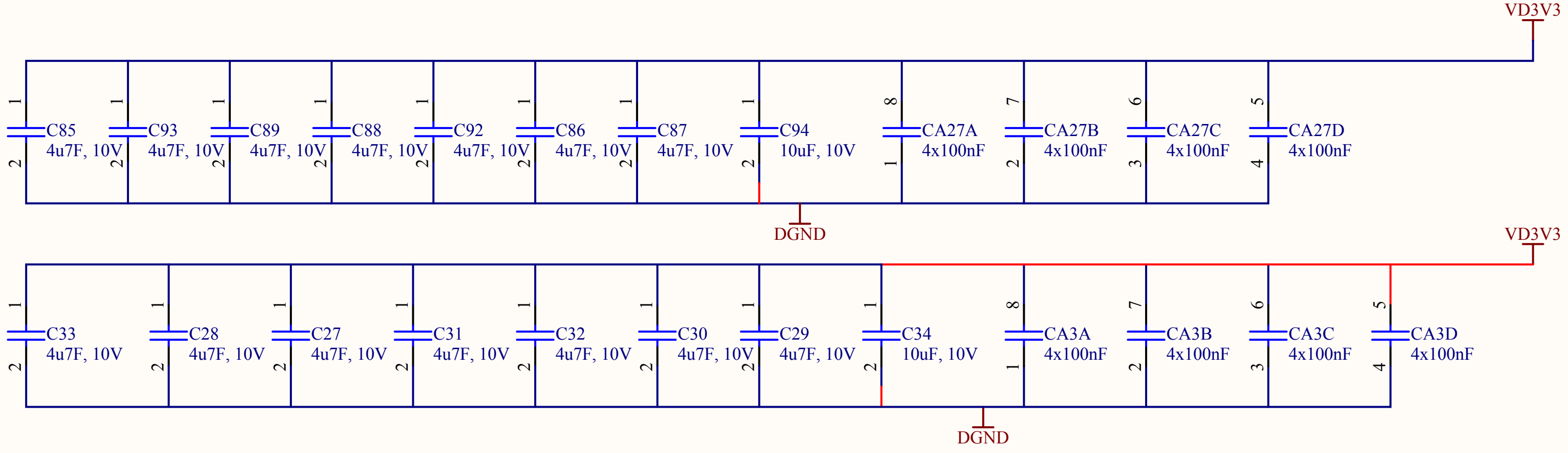
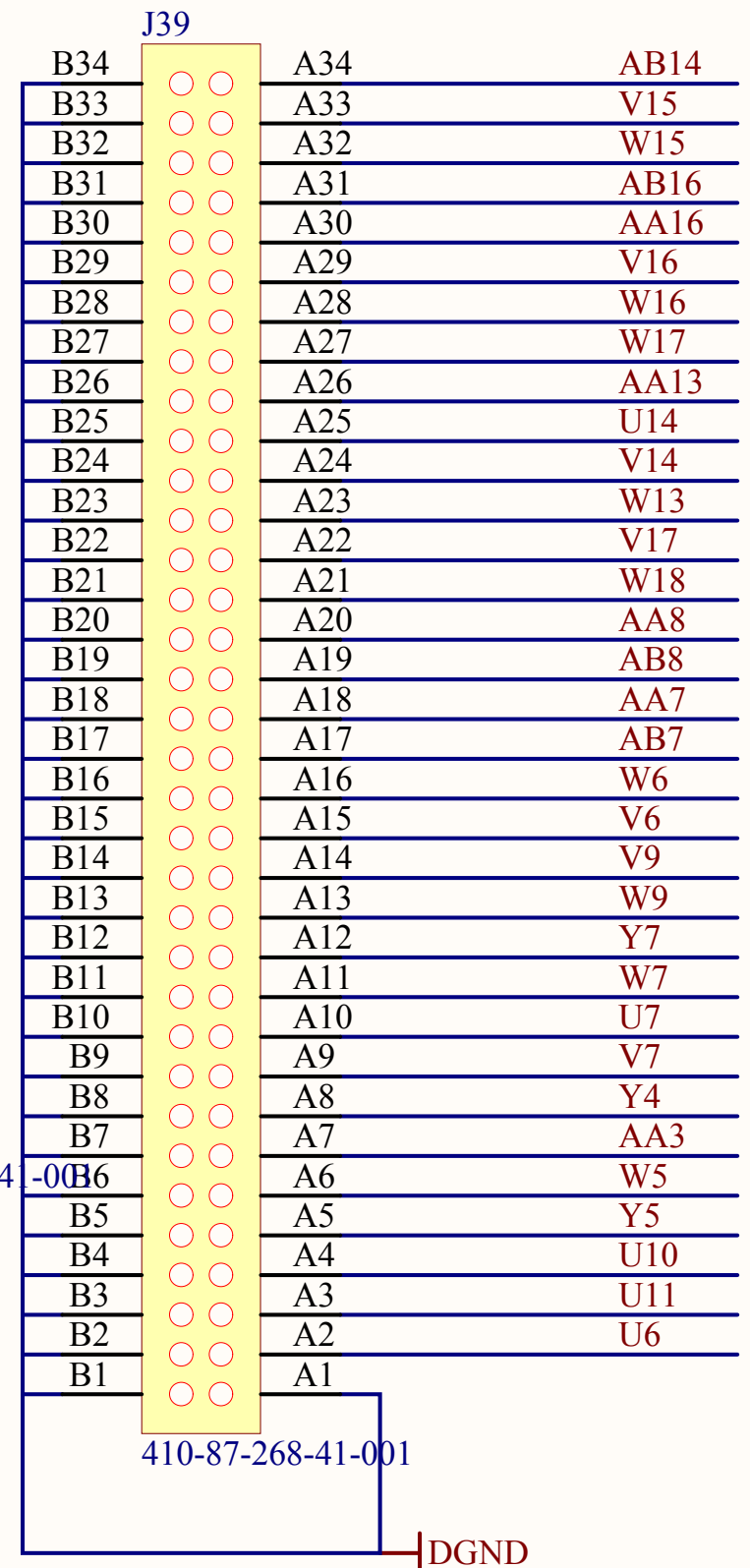
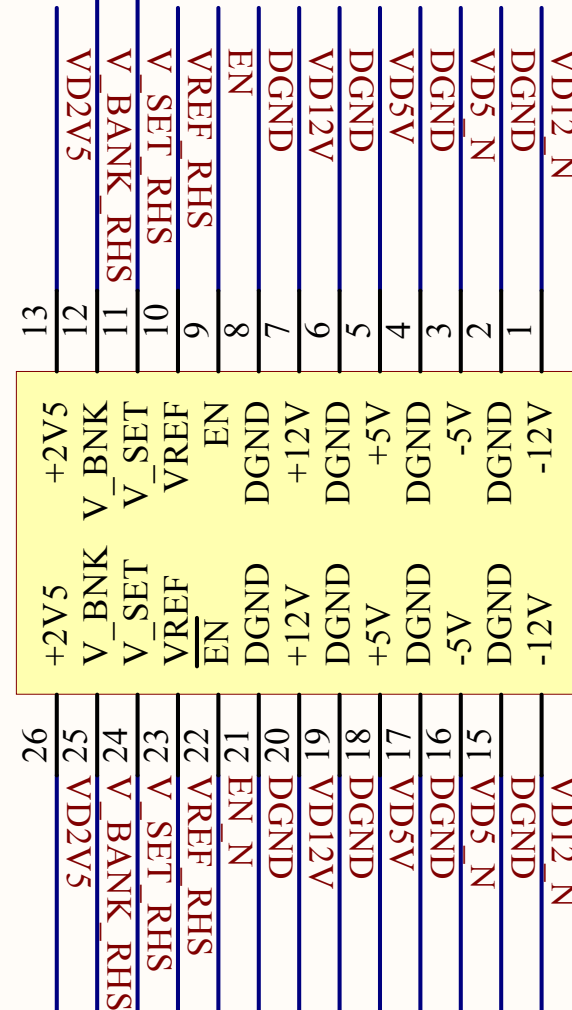
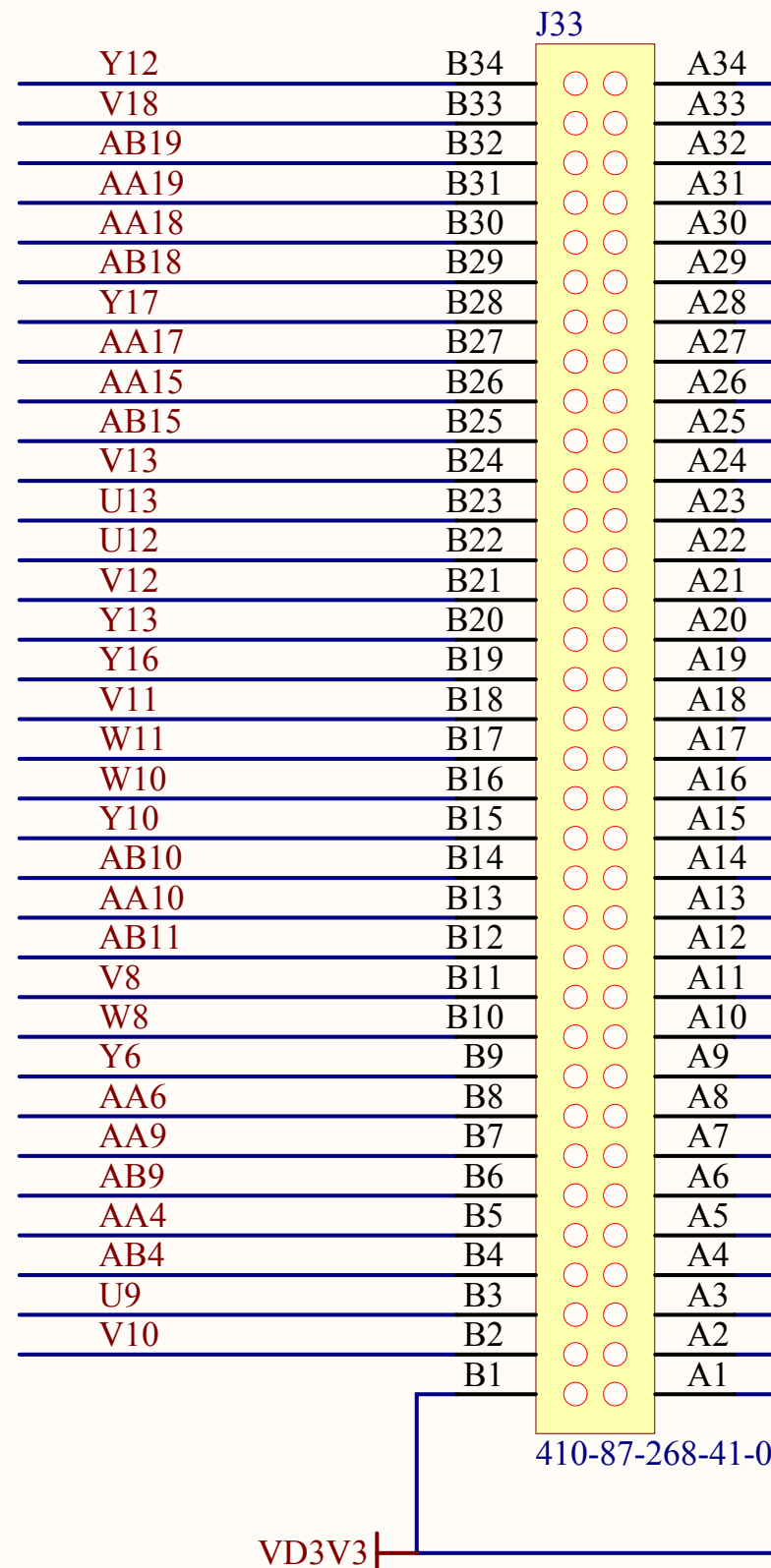
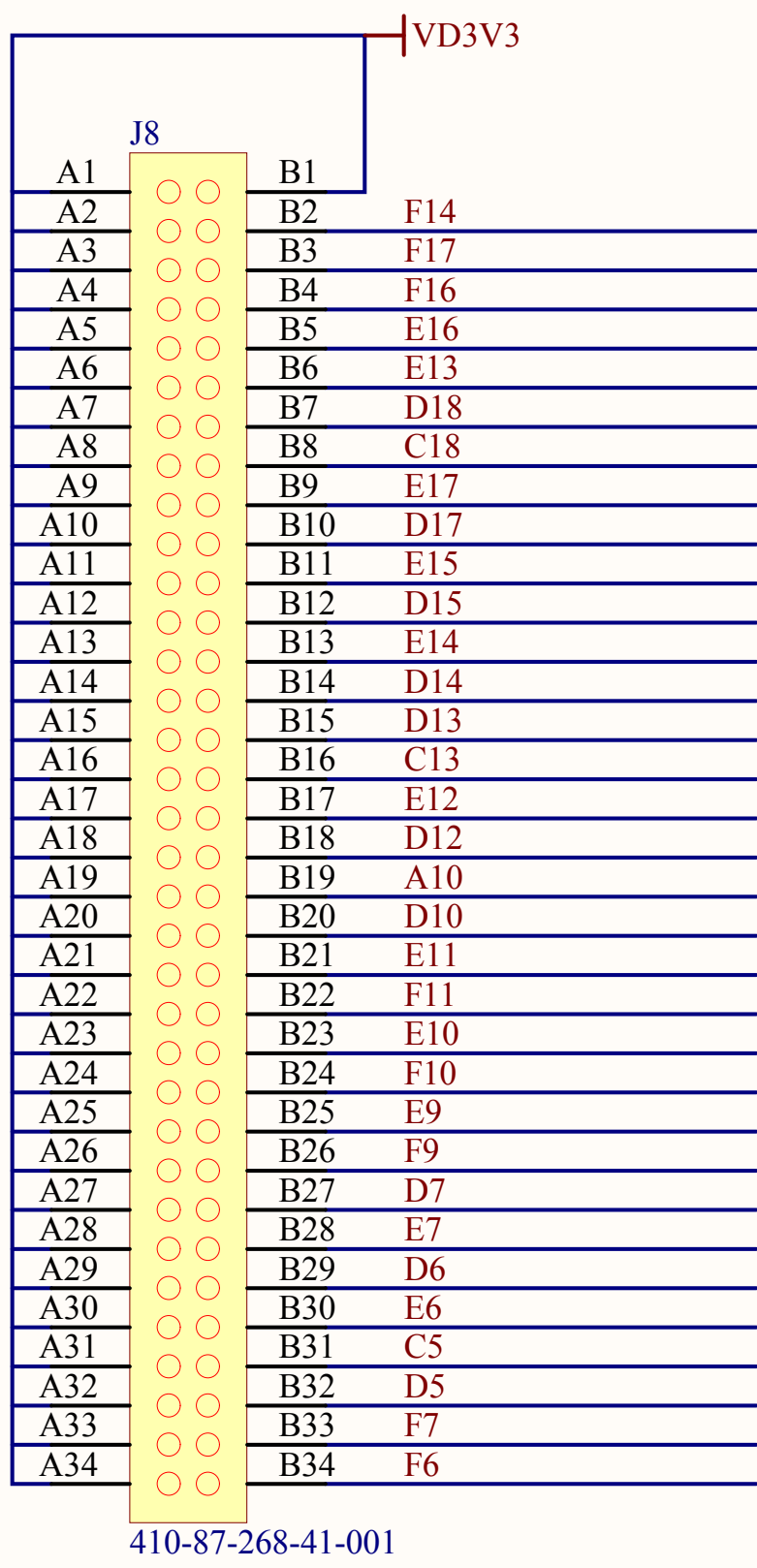
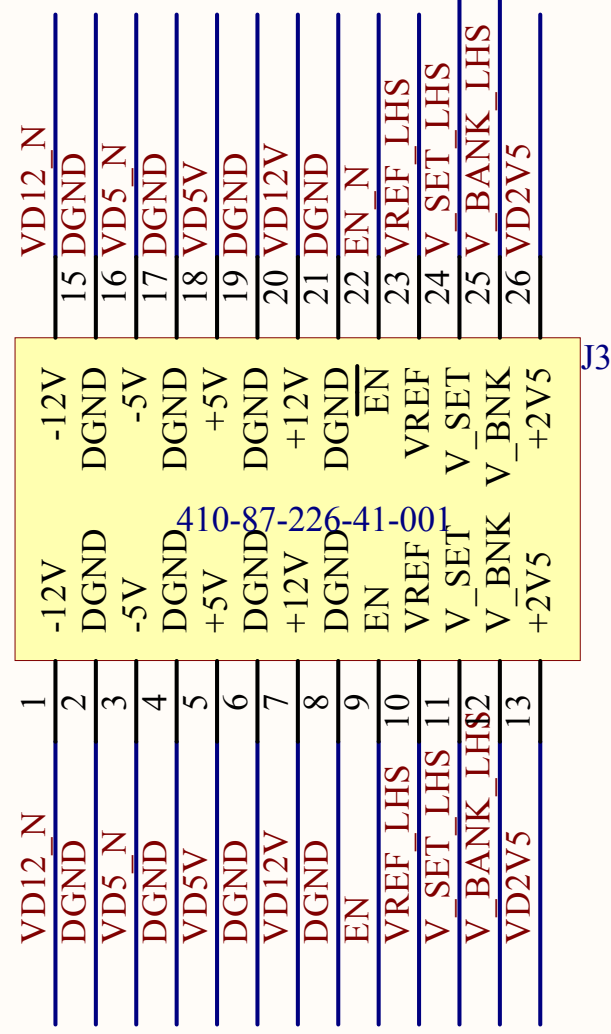
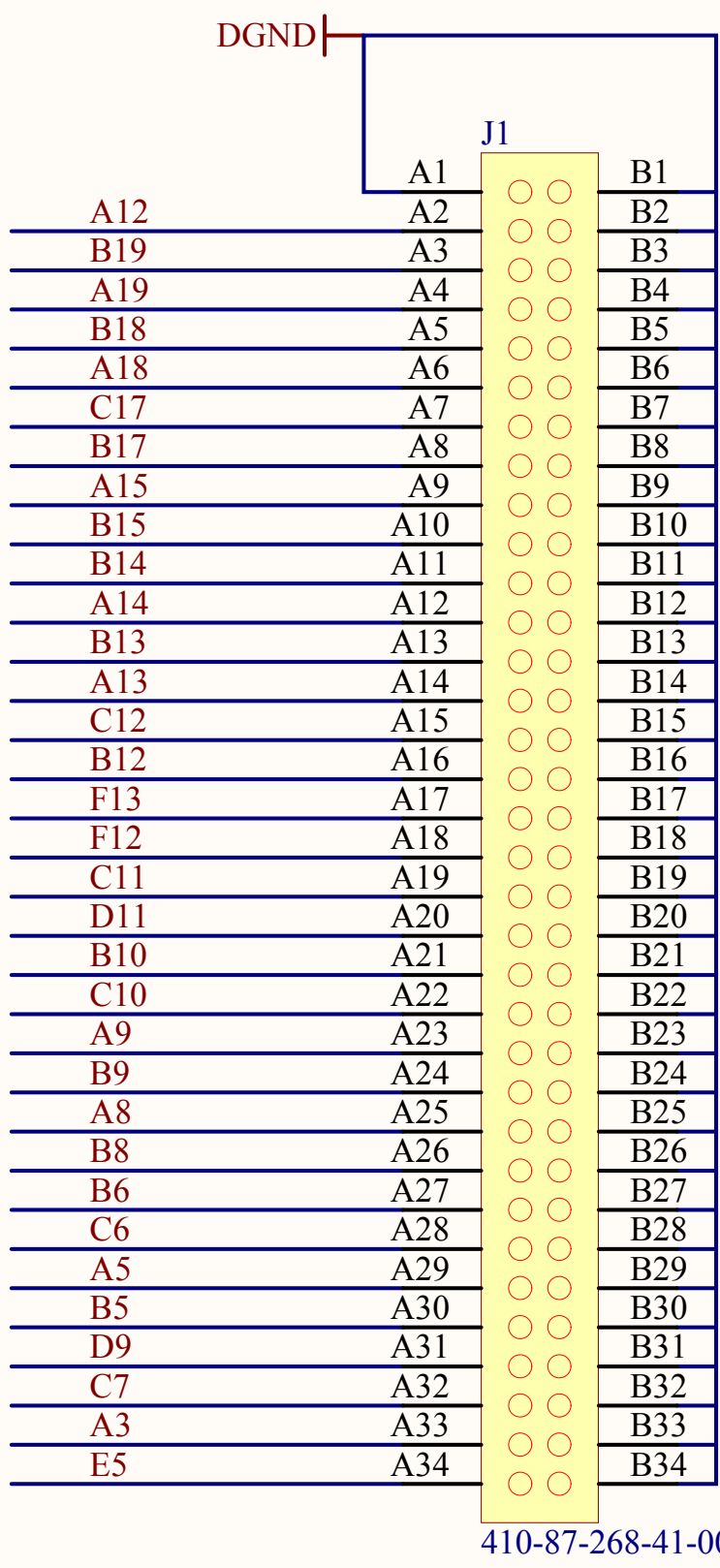
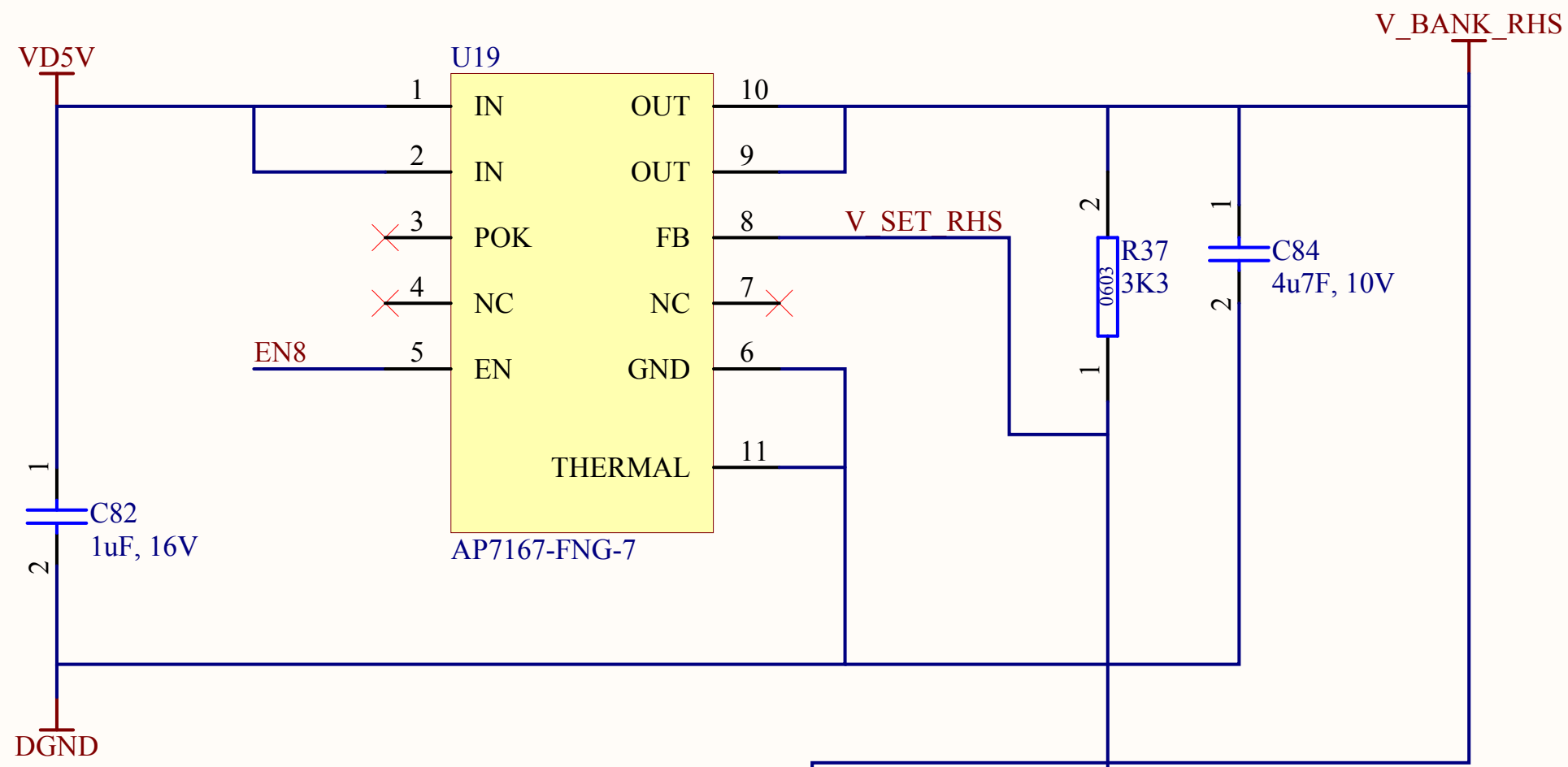
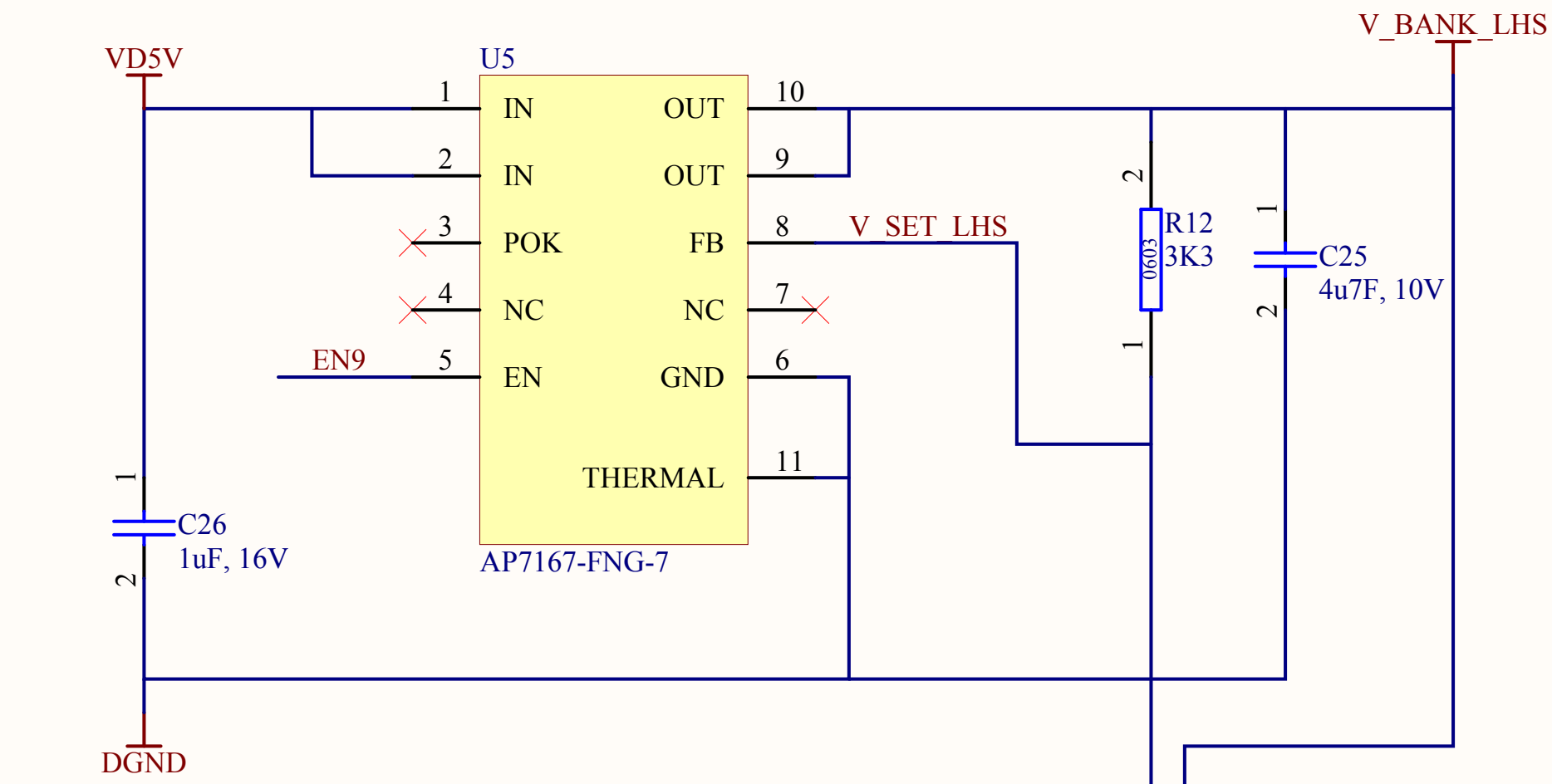
D

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D



A

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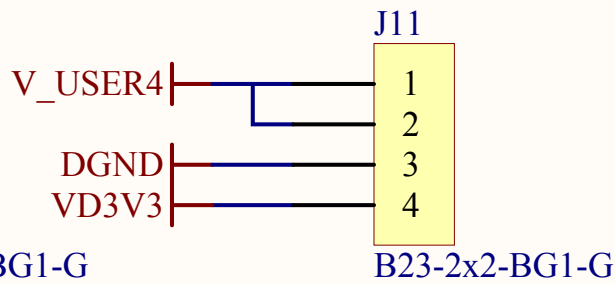
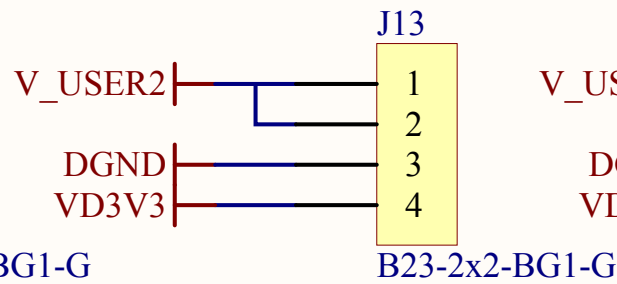
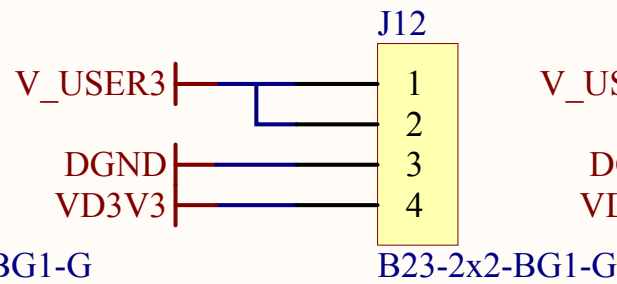
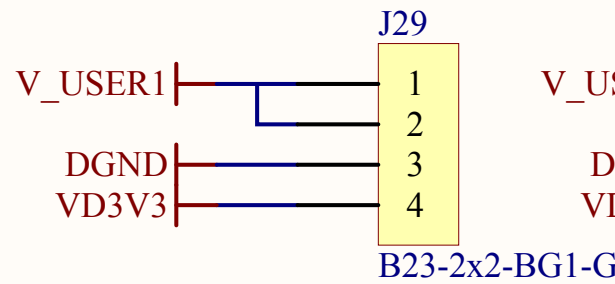
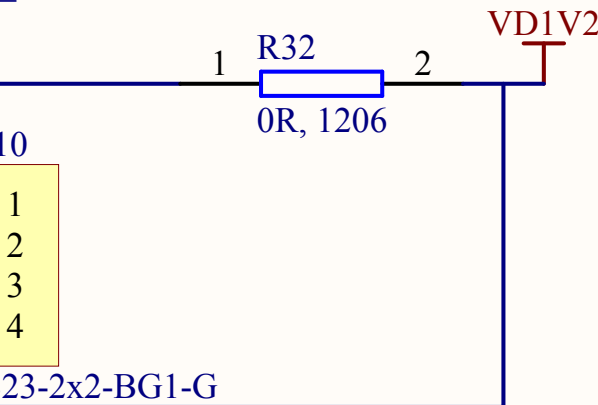
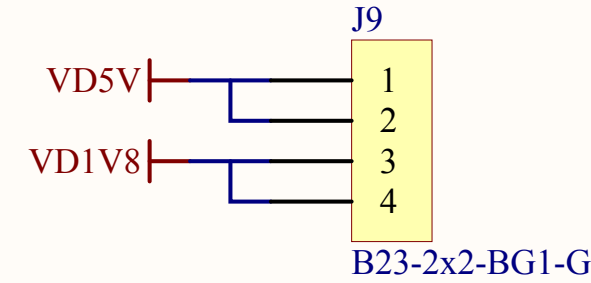
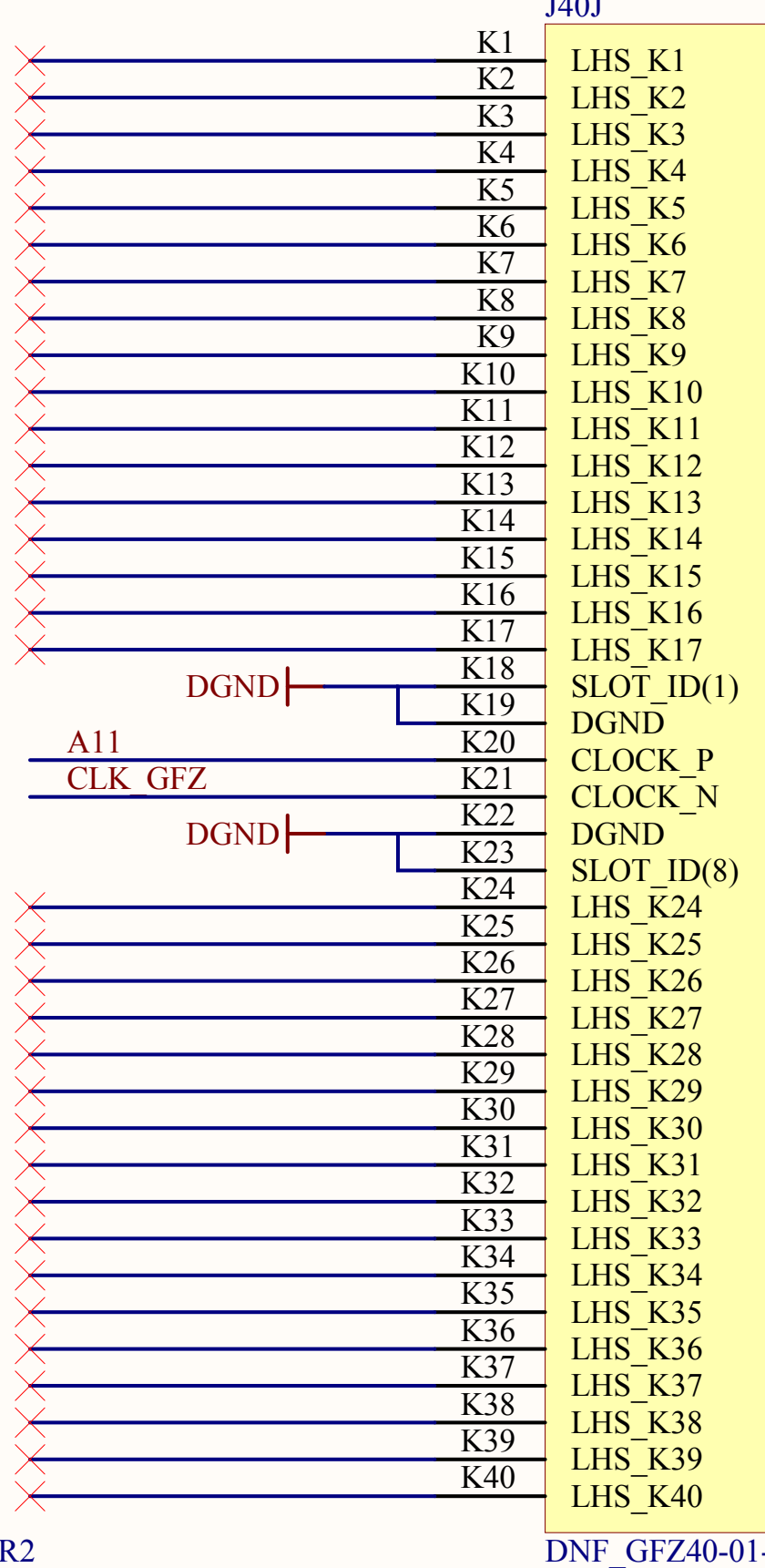
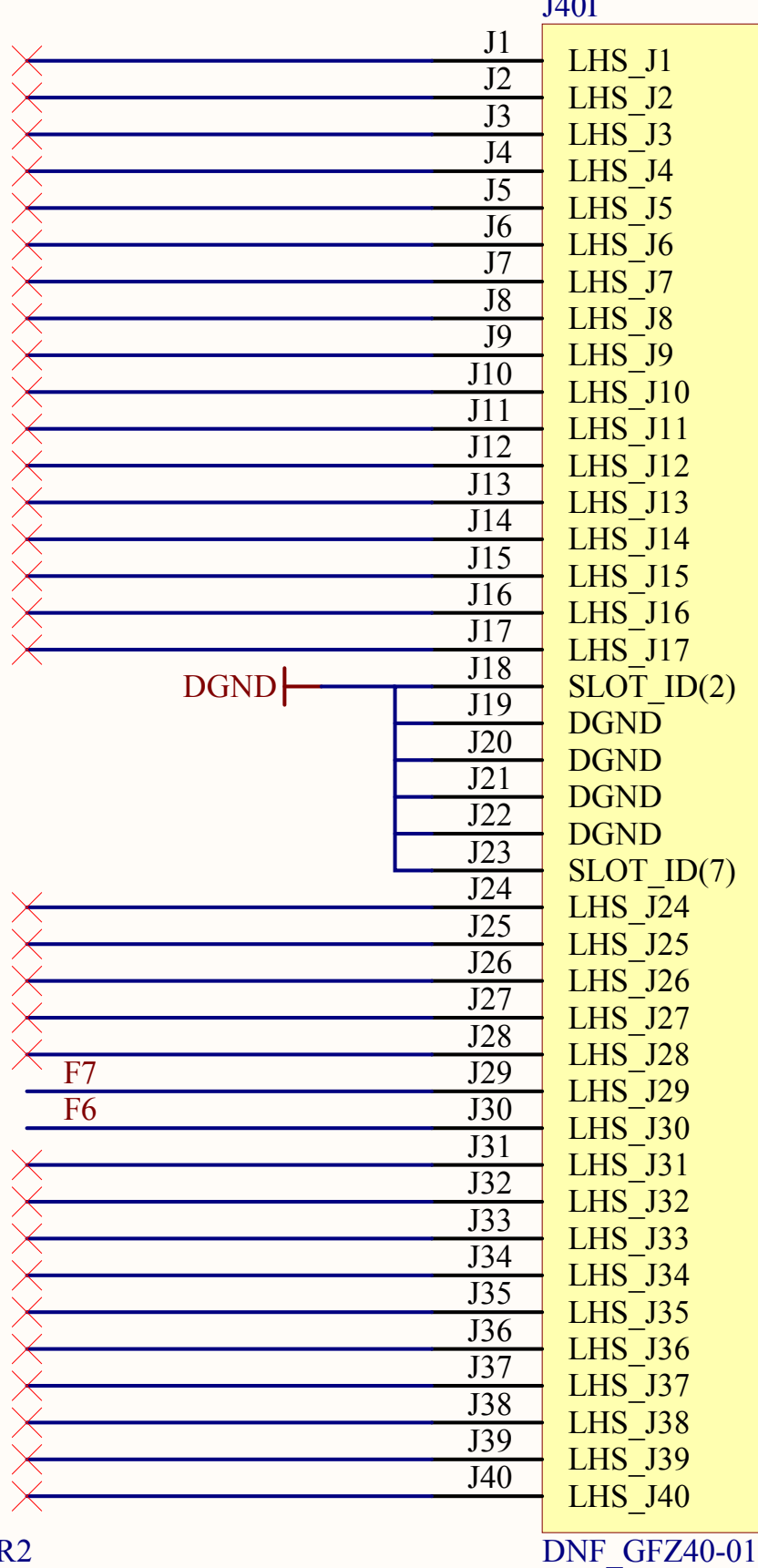
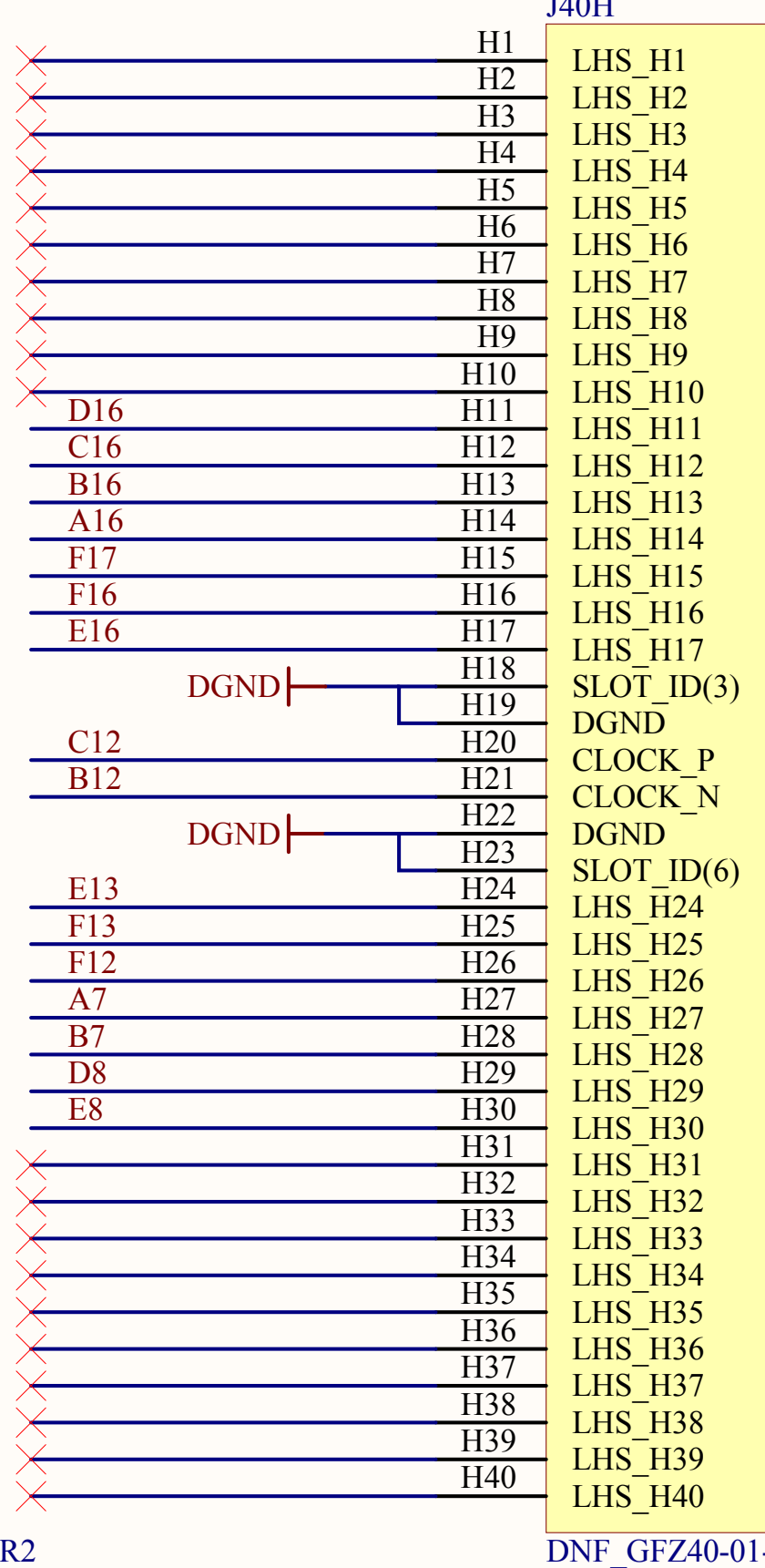
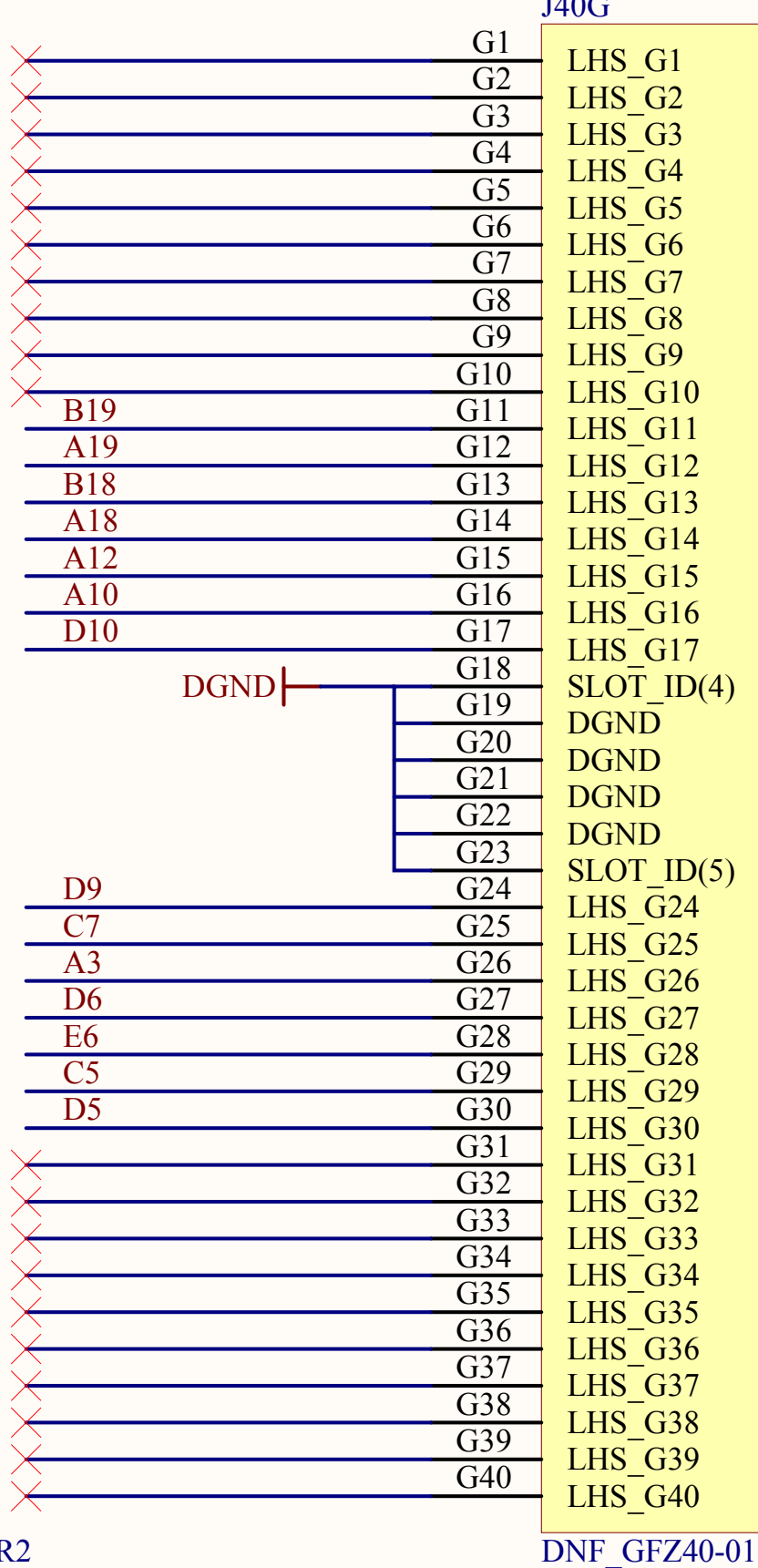
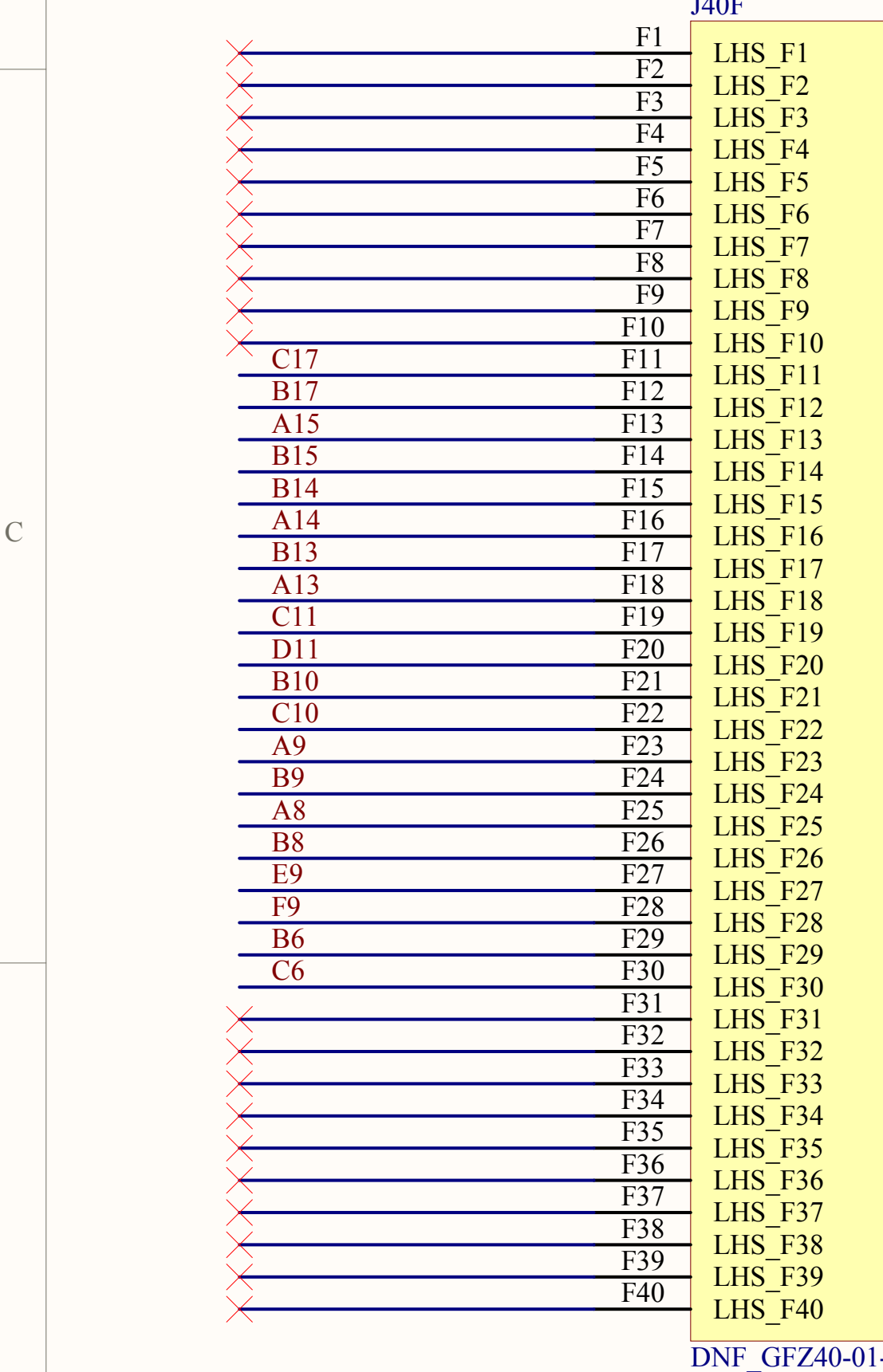
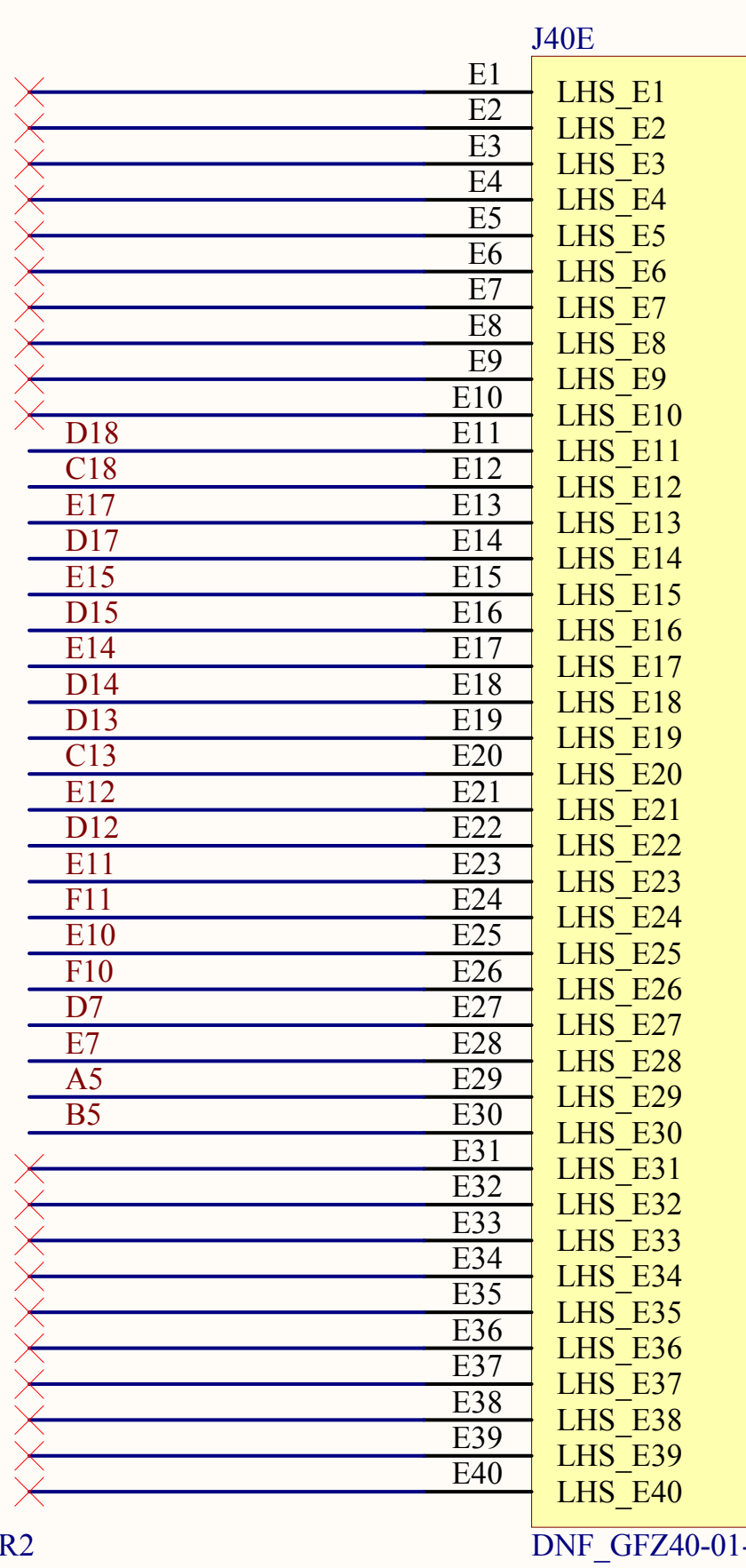
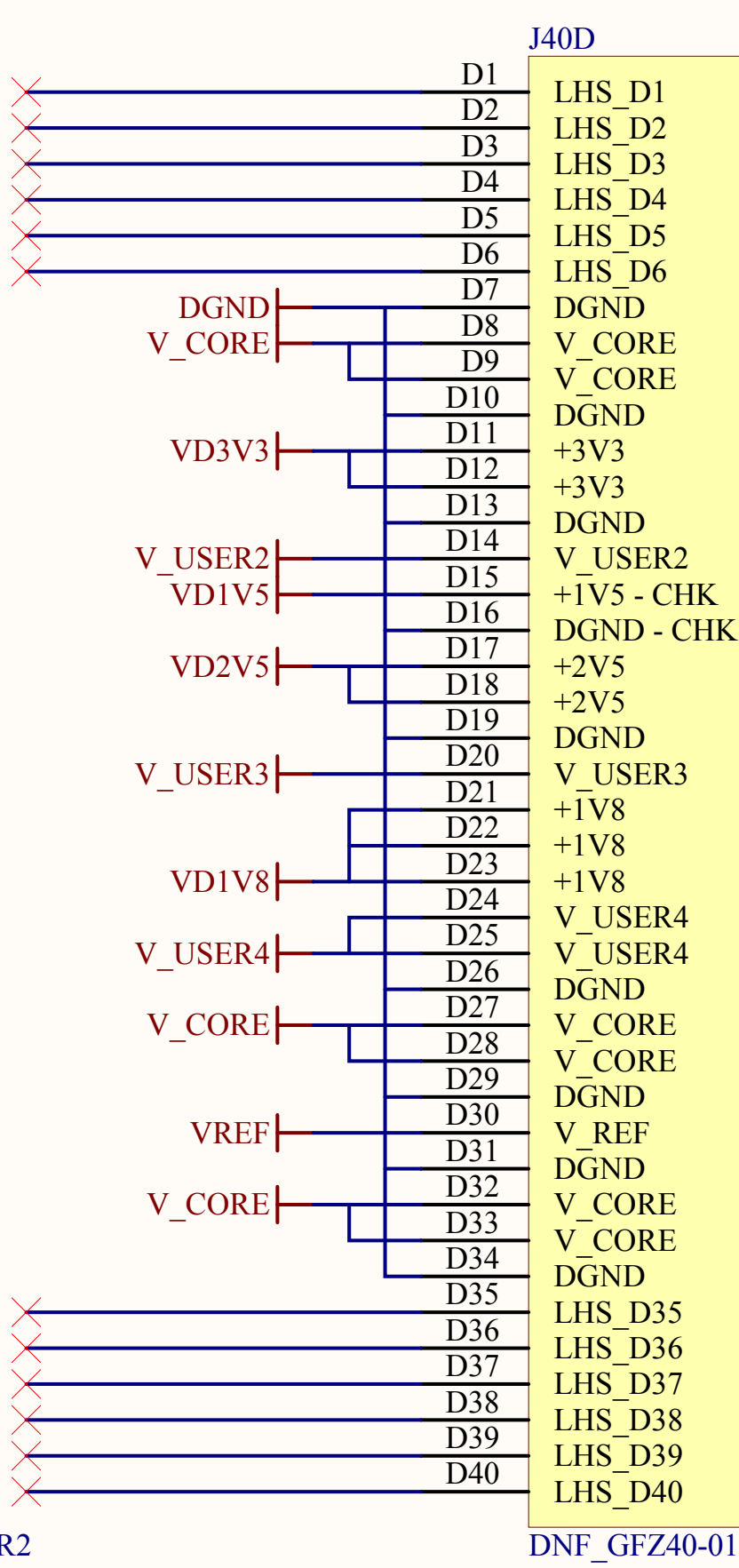
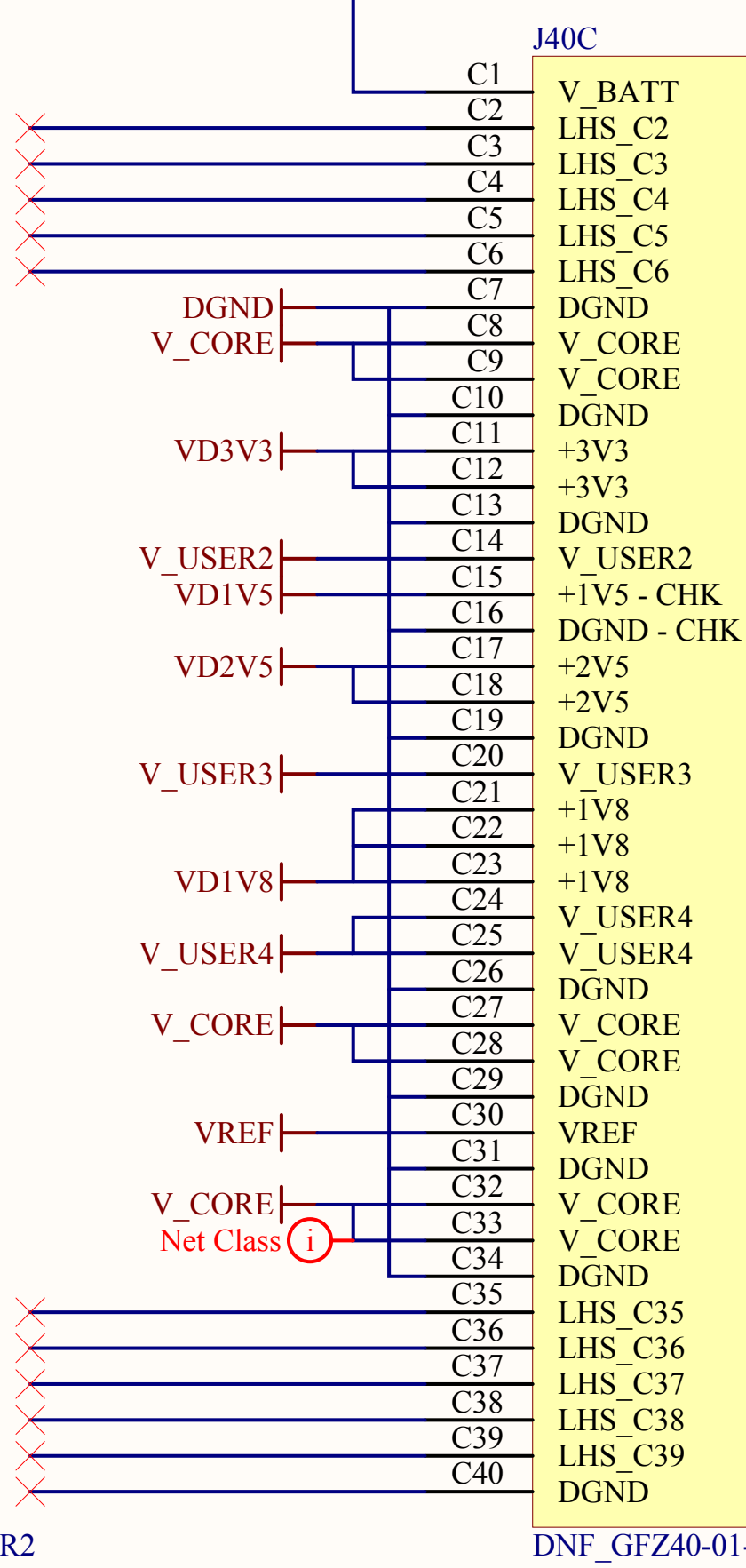
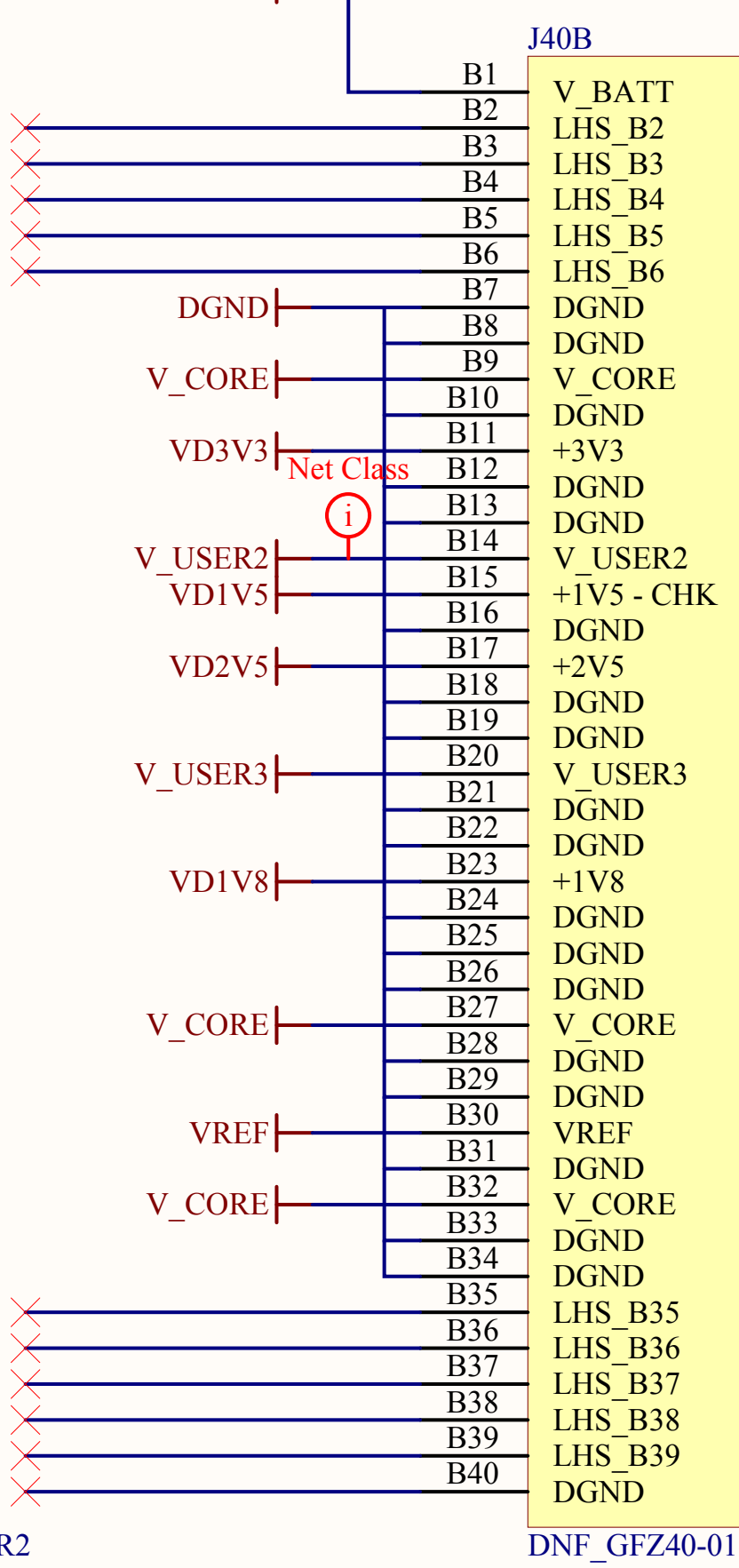
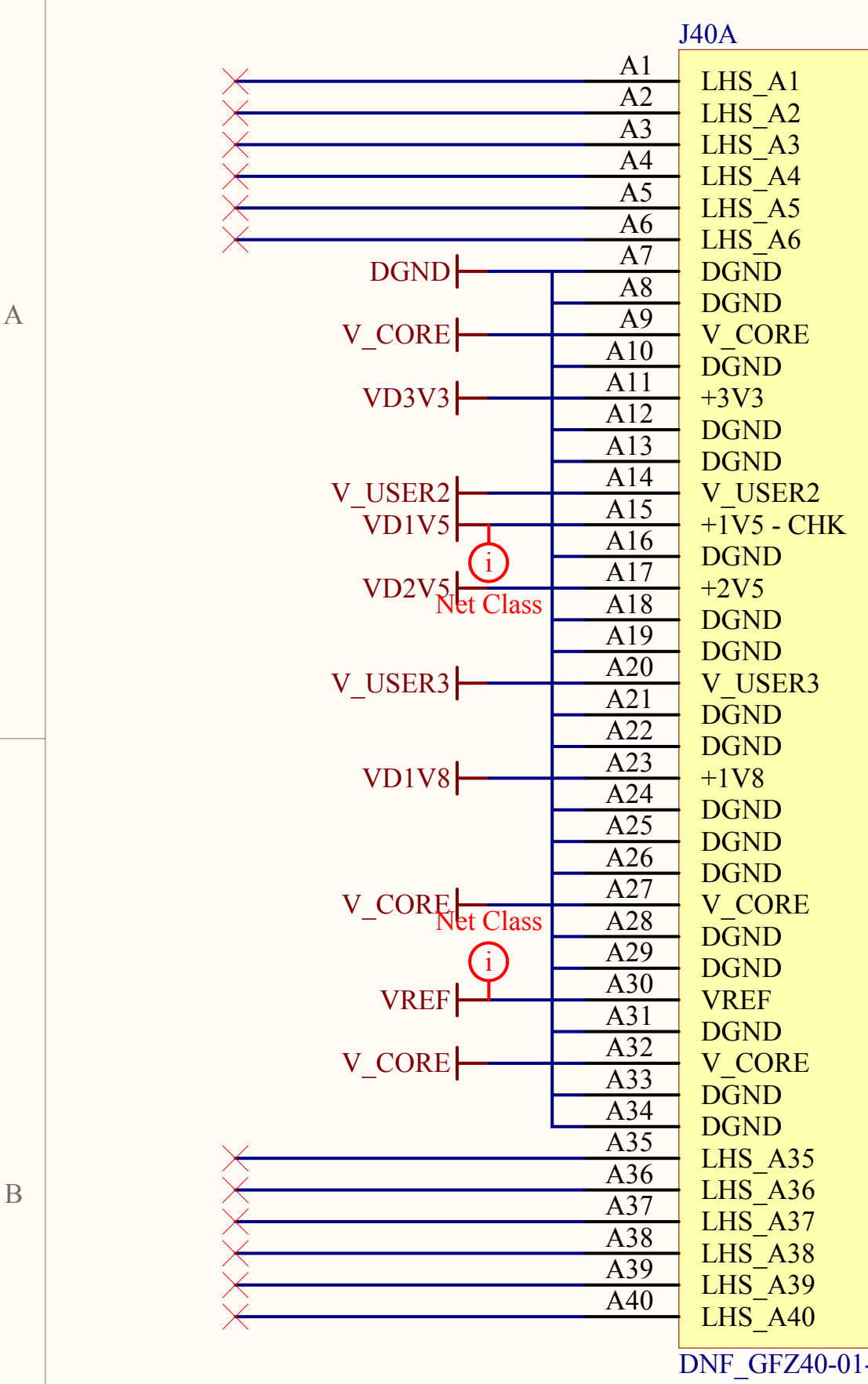
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A

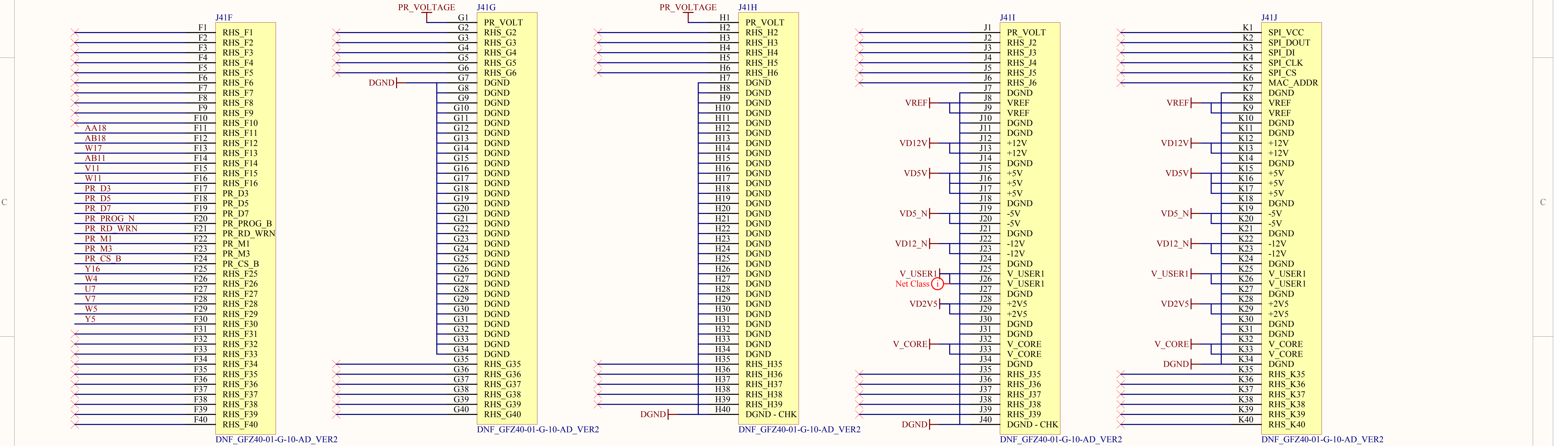
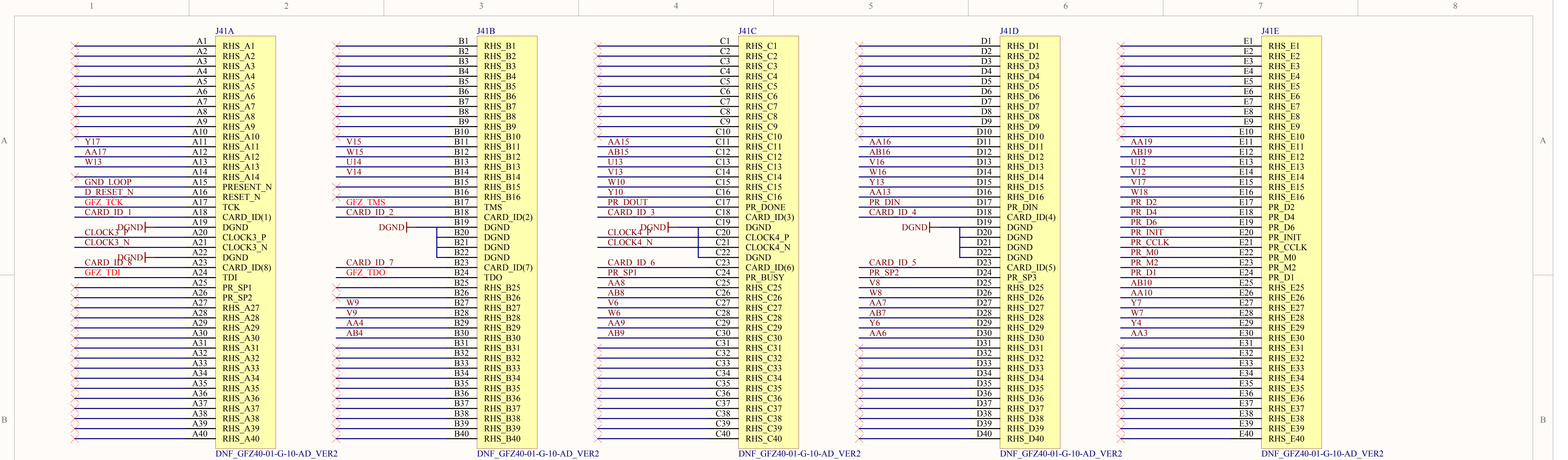
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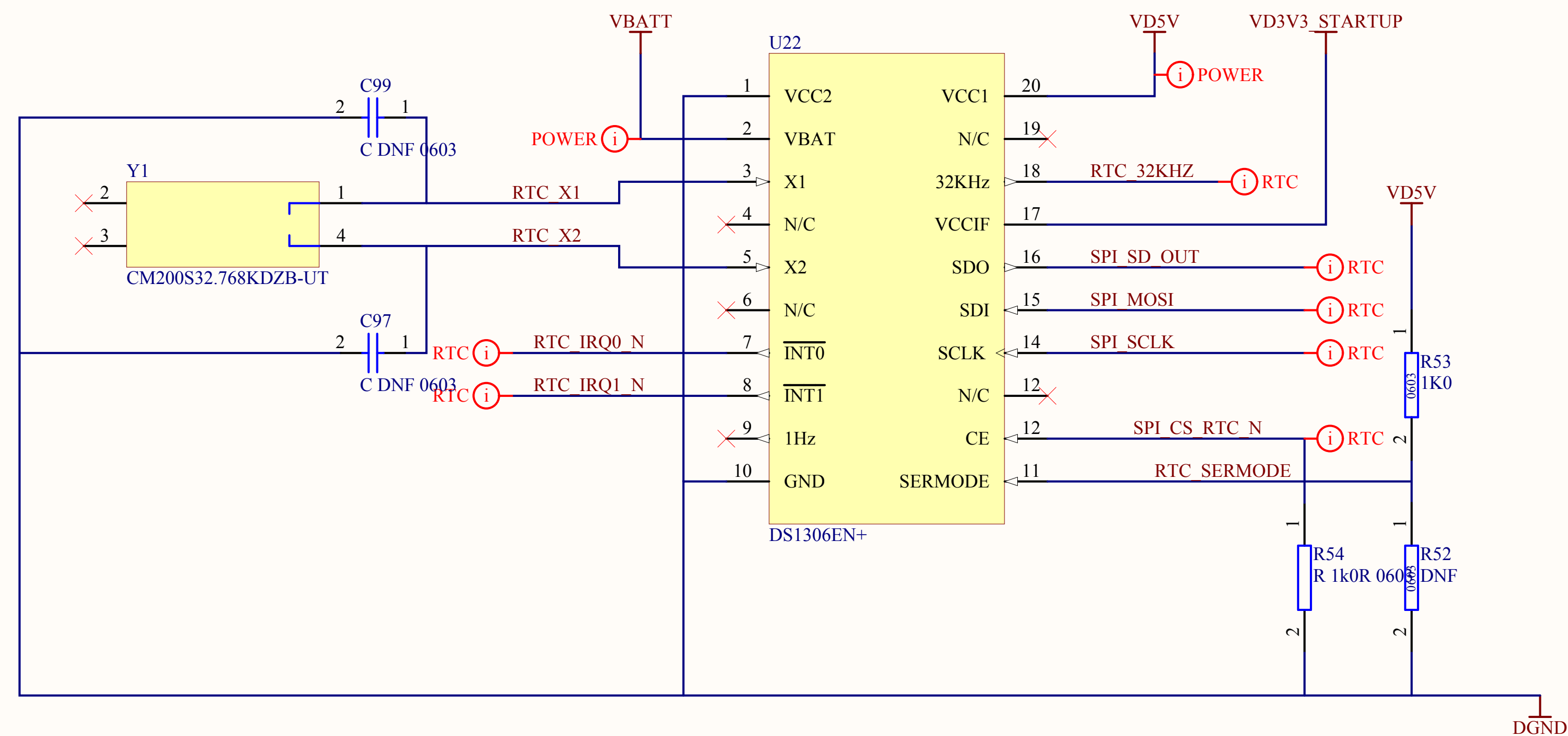
C

D

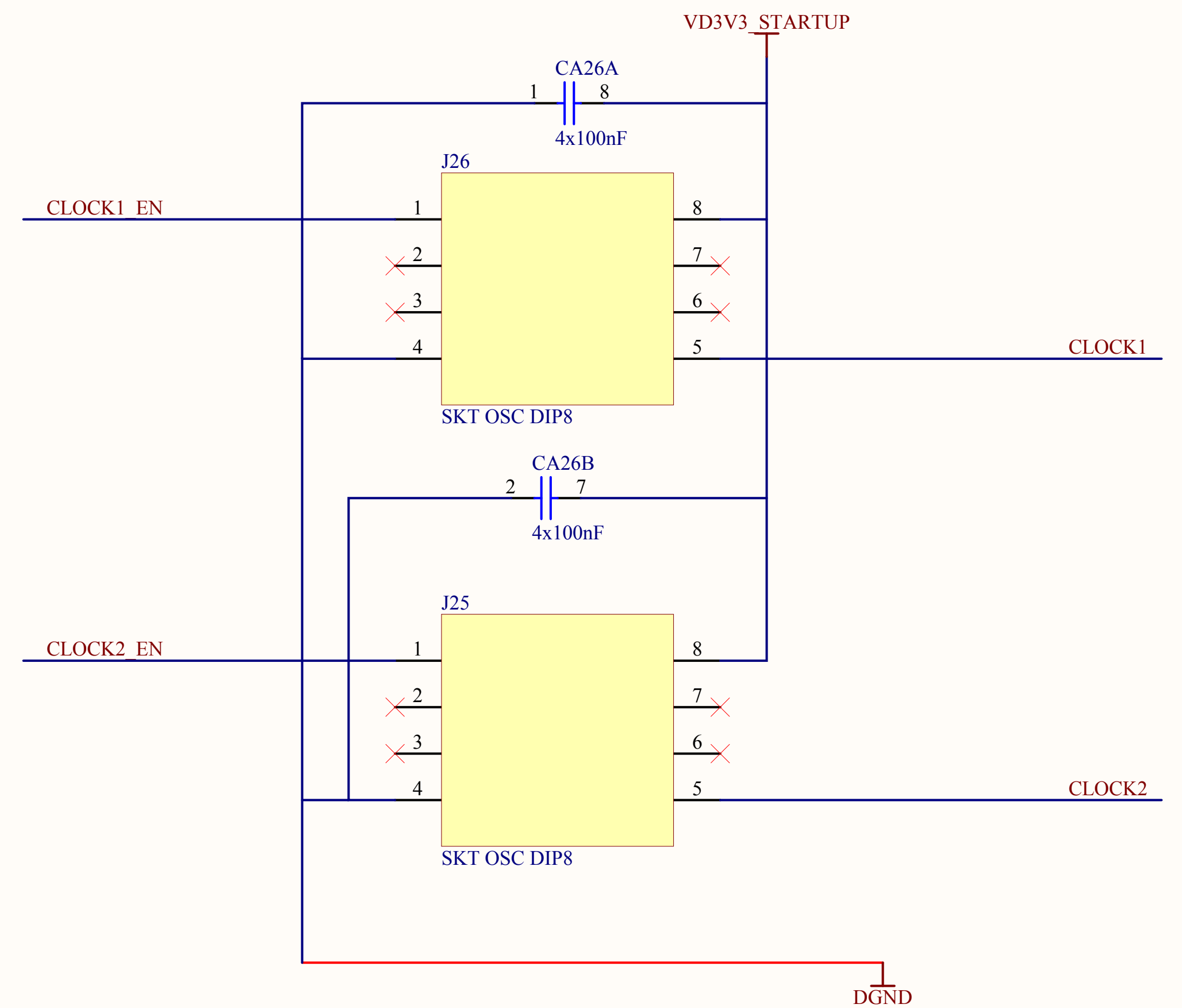
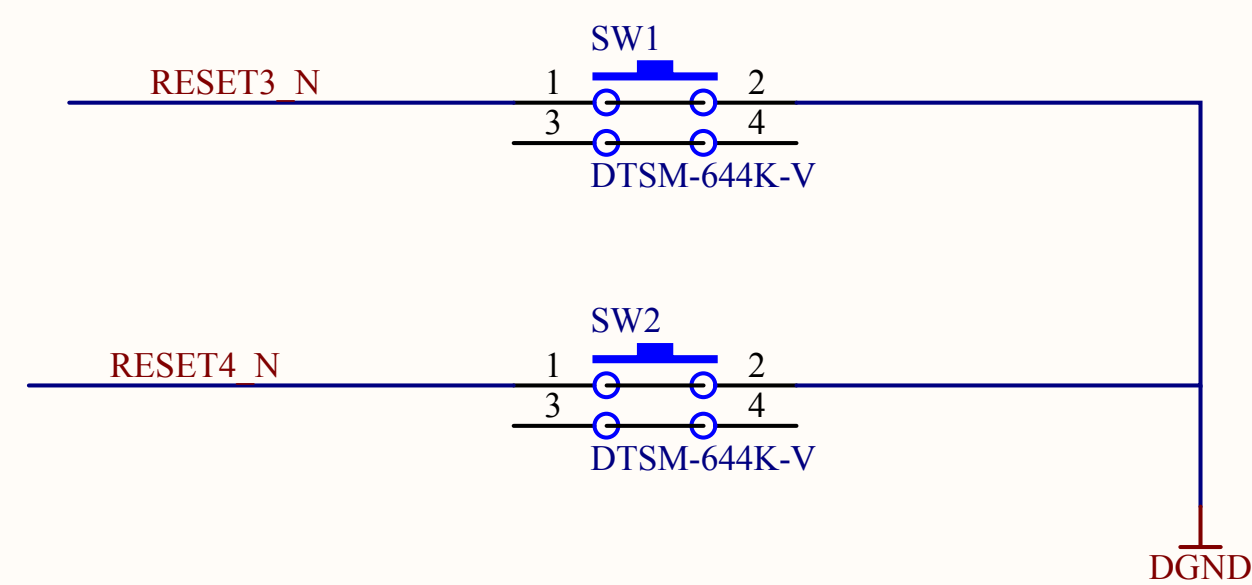
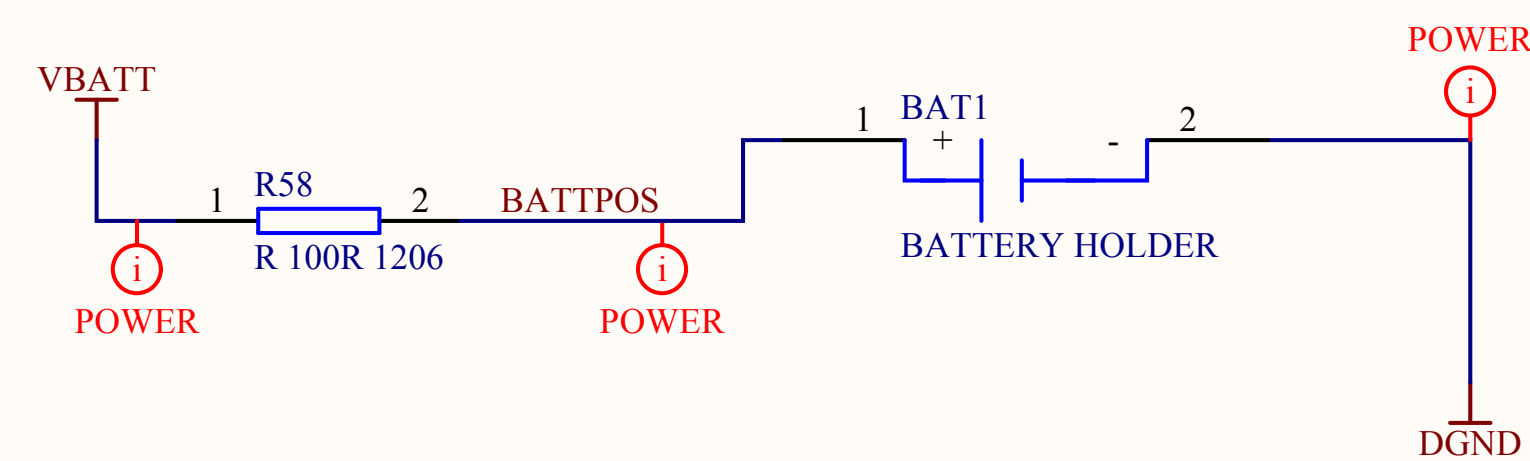


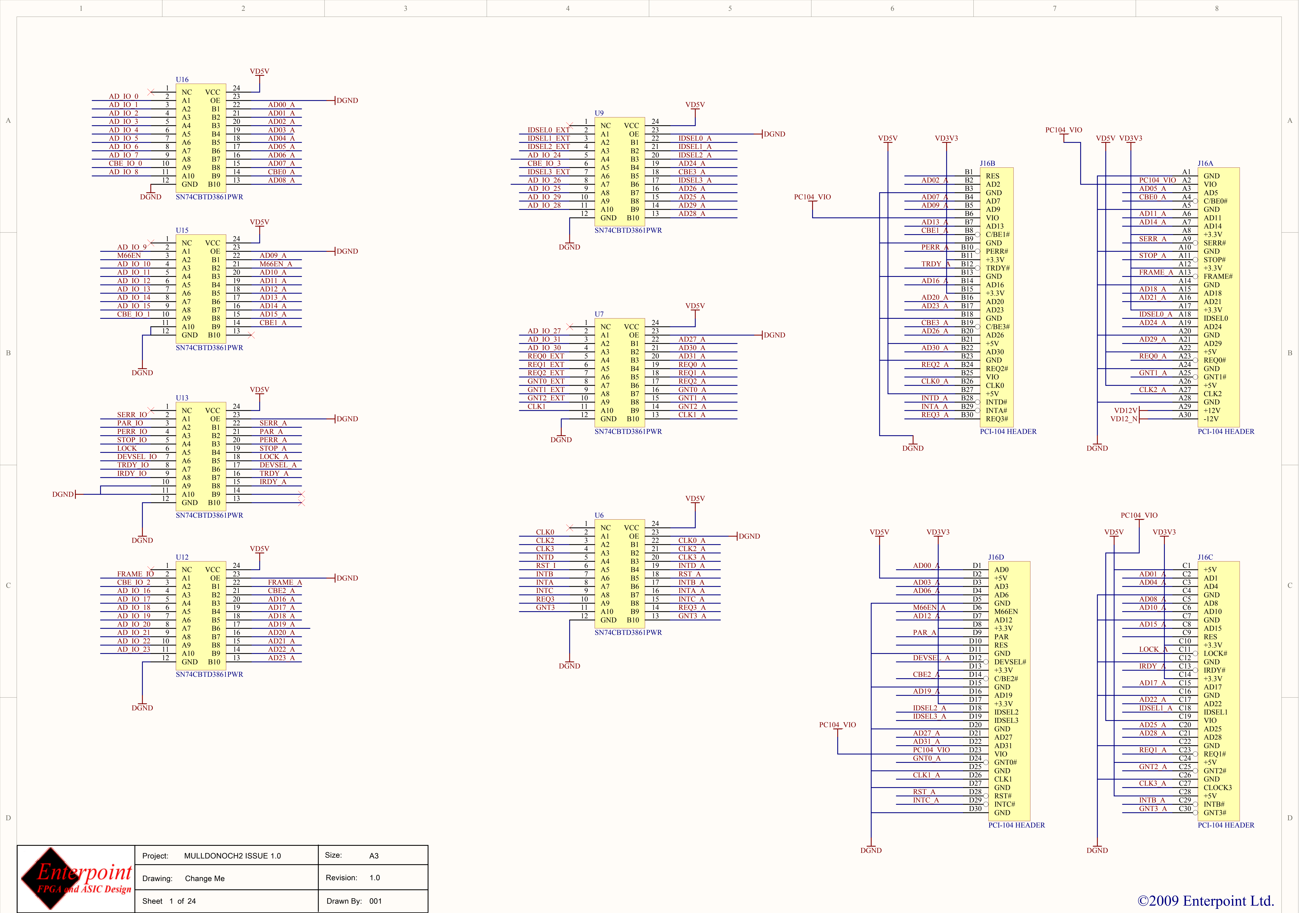
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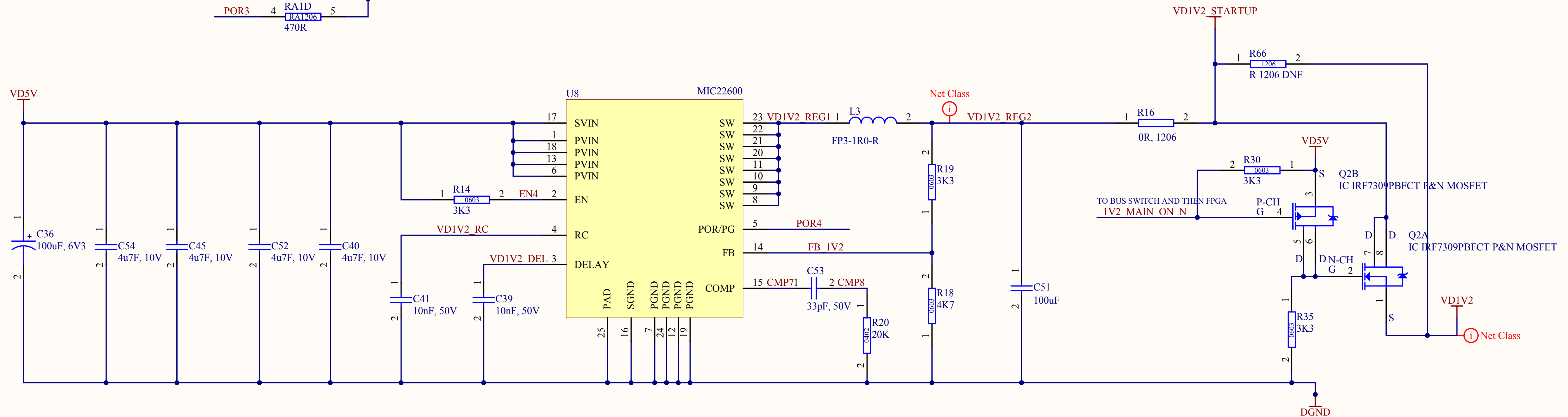
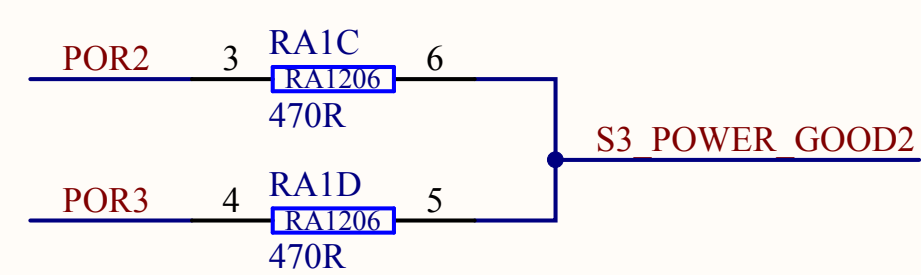
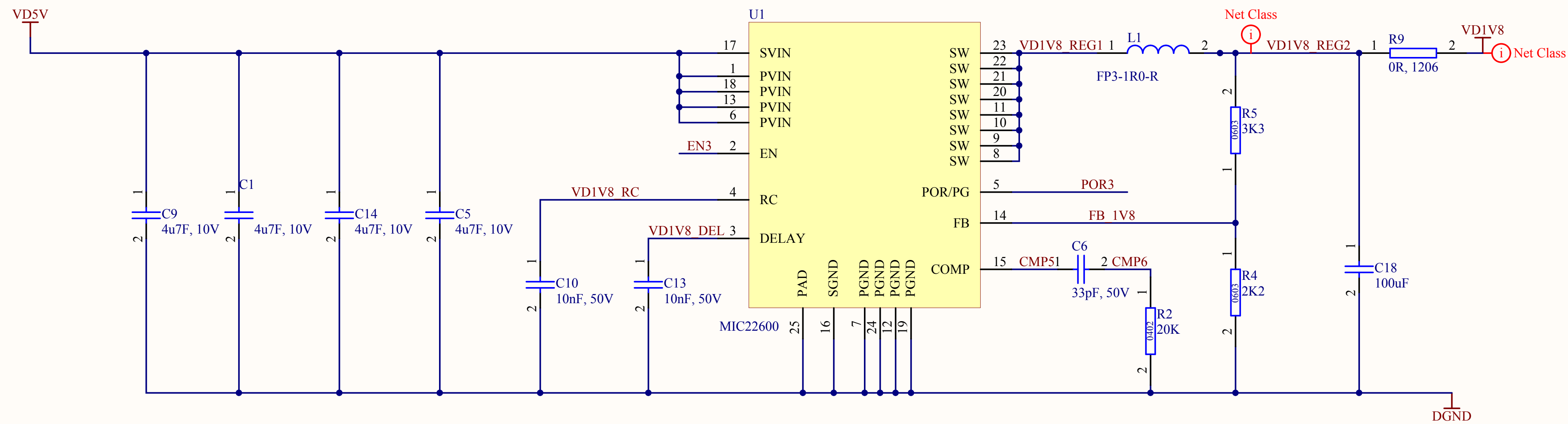


THIS MUST BE SPI SERIAL MODE - CHECK DATA SHEET THEN DELETE r27

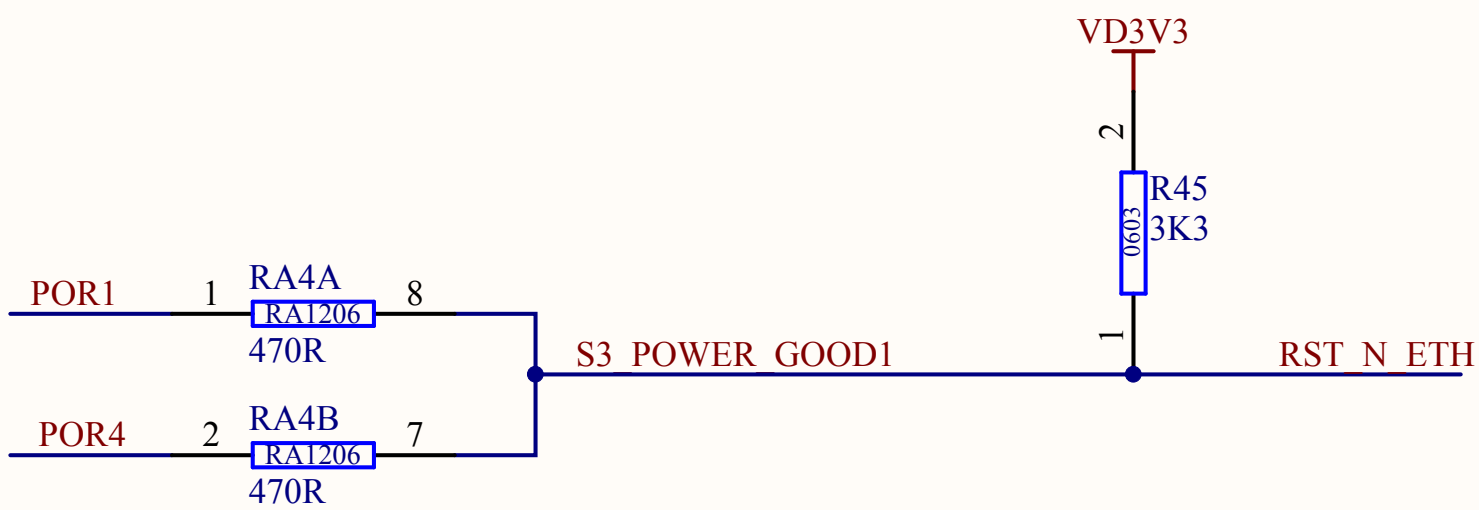
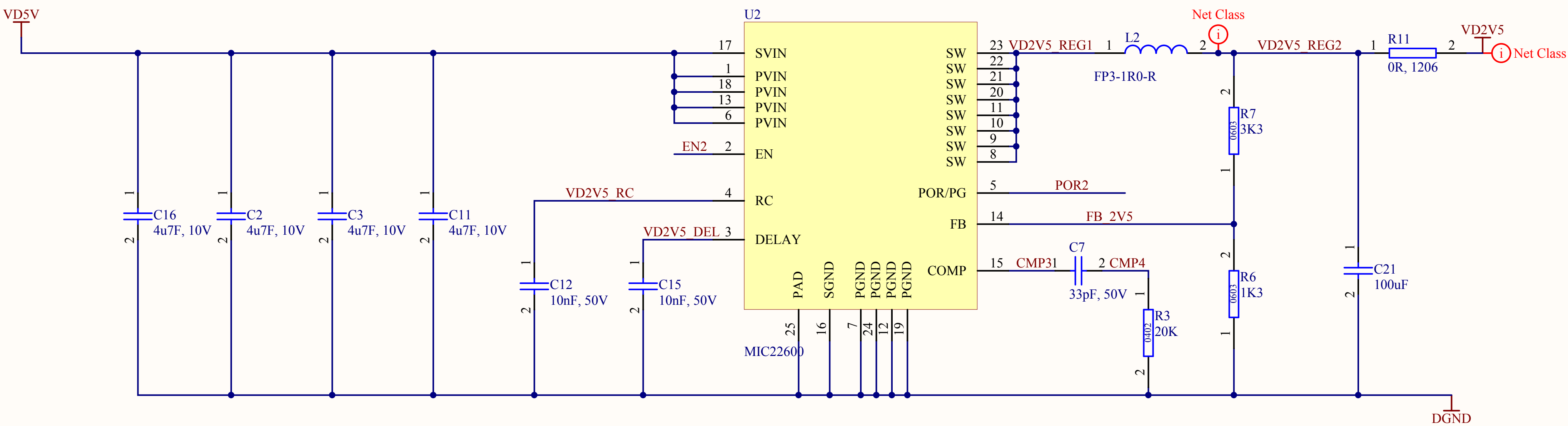
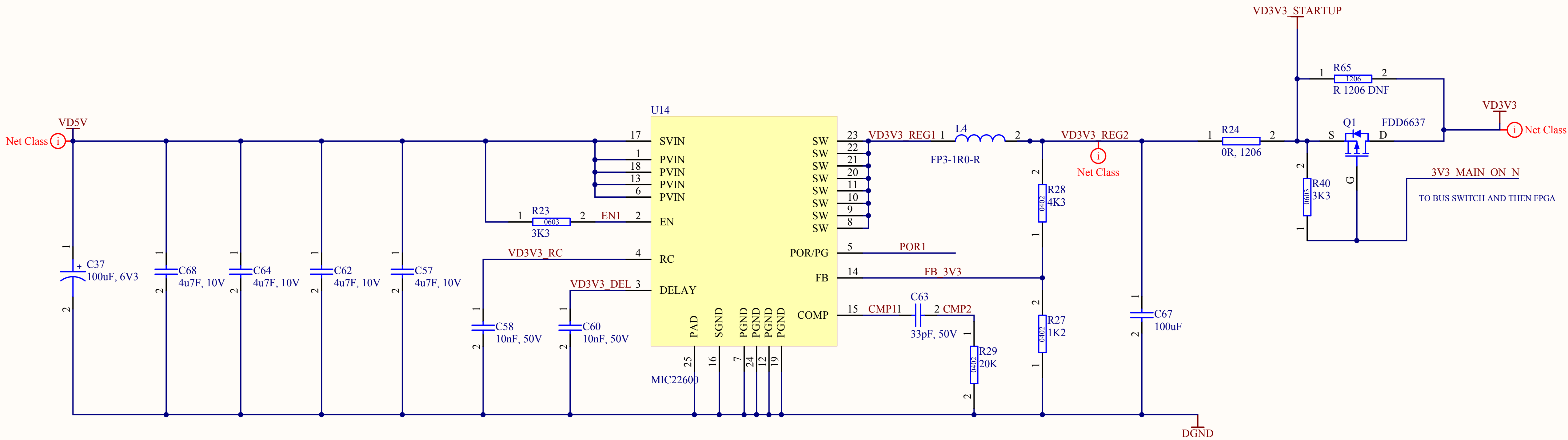


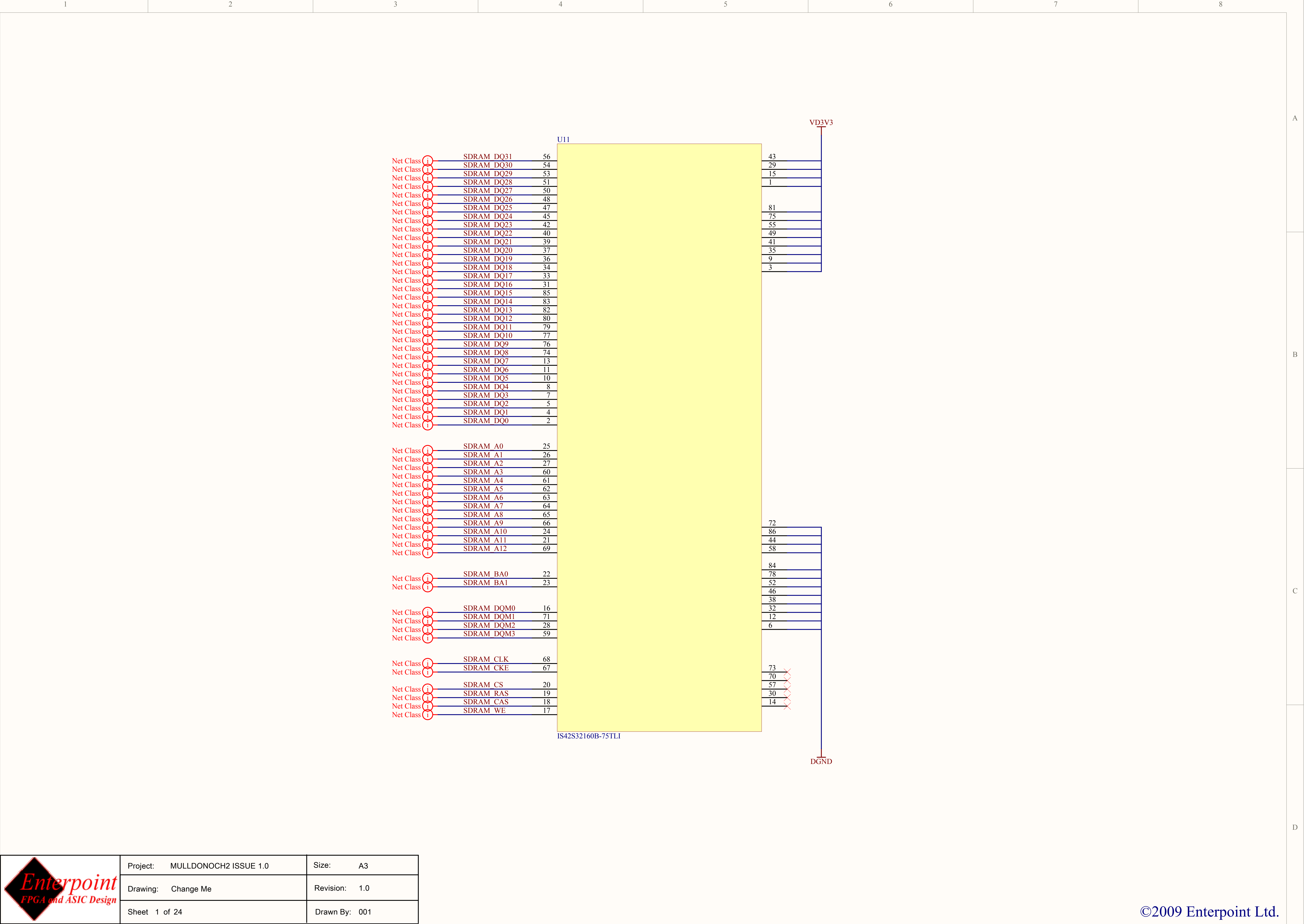


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FPGA and ASIC Design

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Revision:

1.0

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