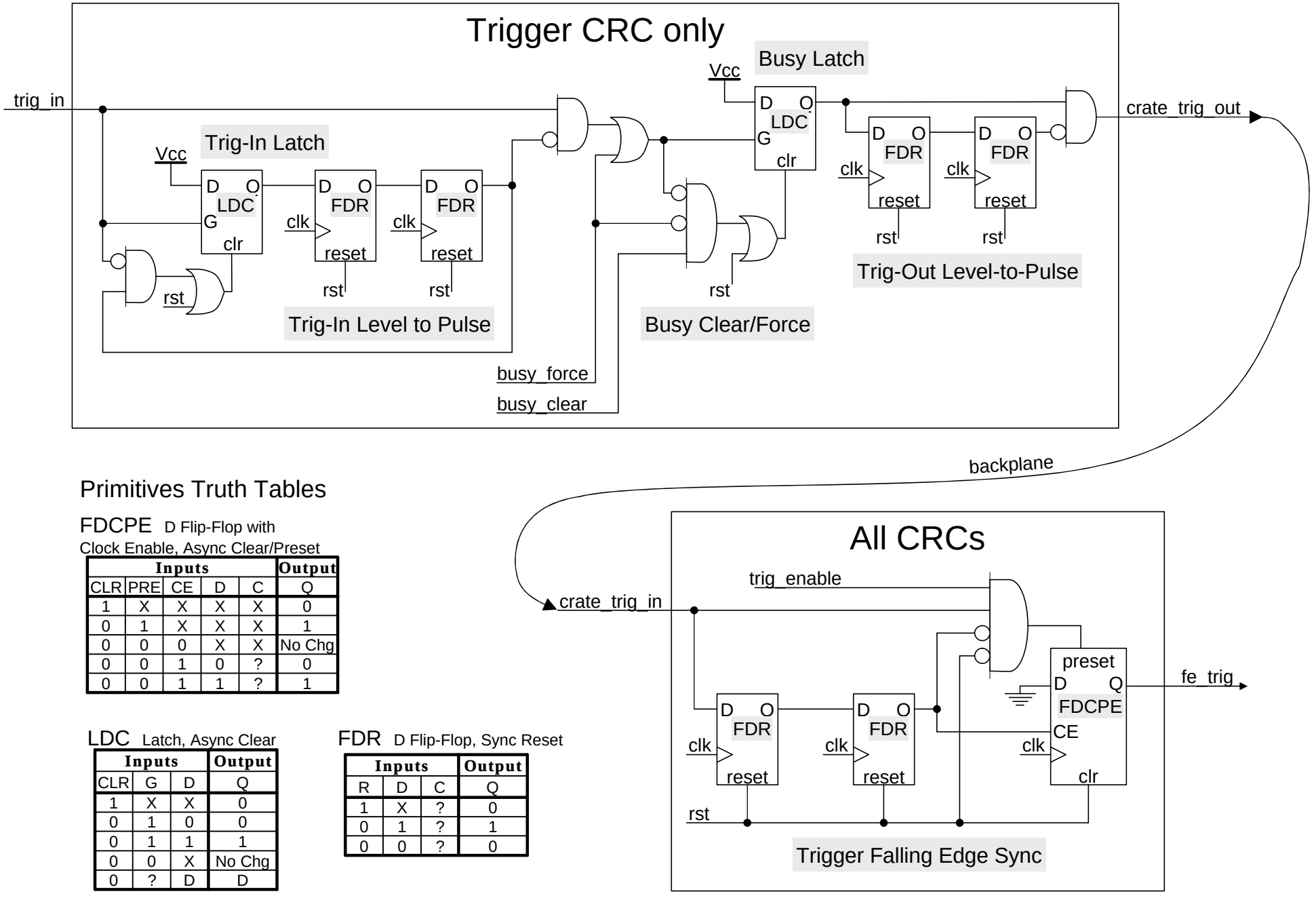

Primitives Truth Tables

FDCPE D Flip-Flop with Clock Enable, Async Clear/Preset

Inputs					Output
CLR	PRE	CE	D	C	Q
1	X	X	X	X	0
0	1	X	X	X	1
0	0	0	X	X	No Chg
0	0	1	0	?	0
0	0	1	1	?	1

LDC Latch, Async Clear

Inputs			Output
CLR	G	D	Q
1	X	X	0
0	1	0	0
0	1	1	1
0	0	X	No Chg
0	?	D	D

FDR D Flip-Flop, Sync Reset

Inputs			Output
R	D	C	Q
1	X	?	0
0	1	?	1
0	0	?	0