Project Specification
Project Name: ABC-N ASIC
Version: V1.1

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PRELIMINARY STATEMENTS ABOUT THE DOCUMENT

This version of the ABC-N specifications is created from the original document describing ABCD3TA, the front-end readout chip used in the present ATLAS Semiconductor Tracker:
ABCD3TA ASIC Requirements and Specification
ATL-IS-ES-0039
EDMS Id: **317413**
https://edms.cern.ch/cedar/plsql/doc.info?cookie=7245285&document_id=317413&version=1
http://scipp.ucsc.edu/groups/atlas/elect-doc/abcd3t_spec.pdf

The readout architecture remains identical; the main changes are listed below:

- 250nm CMOS technology
- 2.5V power supply
- On chip voltage regulators
- Positive or negative input charge
- Register Read function
- Readout clock up to 160Mbits/sec
- Readout mode compatible with an external module controller
- Bonding pads arrangement, chip size fitting to the hybrid prototypes

Other changes include :

- Pipeline length up to 6us
- Derandomizer length up to 42 events
- Overflow mode
- Memory Self Test
- SEU flags
- I/O and register scan through JTAG

The frontend specifications are written for the “short strip” detector model

Comments, open issues, preliminary parameters or descriptions are printed in grey in this document.

1 SCOPE

This document describes the requirements and target design specifications for the front-end ASIC to be used in the binary readout architecture of silicon strip detectors in the ATLAS Semiconductor Tracker Upgrade. The ABC-N chip is designed firstly in the IBM CMOS6 250nm technology, then a second version in 130nm technology will be developed. The ABC-N design is based upon the ABCD3T-A chip used in the ATLAS SCT Tracker.

2 REFERENCE DOCUMENTS

1. Atlas Binary Chip (ABC), Project Specification, Version V4.03.
2. ABCD3TA ASIC Requirements and Specification, ATL-IS-ES-0039, EDMS Id: 317413
3. RAL 214 /DORIC3 Project Specification, V1.01.
4. RAL 216/LDC Project Specification, V 1.01.
5. F. Campabadal, et al., “Design and performance of the ABCD3TA ASIC for readout of silicon strip detectors in the ATLAS semiconductor tracker”, Nucl. Instr. and Meth. A 552 (2005), 292-328.
6. J. Kaplon and W. Dabrowski, “Fast CMOS Binary Front End for Silicon Strip Detectors at LHC Experiments”, IEEE Trans. Nucl. Sci. TNS 52, No. 6 (2005), 2713-2720.
7. F. Anghinolfi, W. Dabrowski, Proposal to develop ABC-Next, a readout ASIC for S-ATLAS Silicon Tracker Module Design,
8. F. Anghinolfi, W. Dabrowski, A. Grillo, J. Kaplon, M. Weber, T. Weidberg, Proposal to develop ABC-Next, a readout ASIC for S-ATLAS Silicon Tracker Module Design: Technical Part
9. Technical Specification: Supply of SiliconMicrostrip Sensors of ATLAS07 specification. July 2007.

3 TECHNICAL ASPECTS

3.1 Requirements

3.1.1 General

The chip must provide all functions required for processing of signal from 128 strips of a silicon strip detector in the ATLAS experiment employing the binary readout architecture. The simplified block diagram of the chip is shown in figure 3.1. The main functional blocks are: front-end, input register, pipeline, derandomizing buffer, command decoder, readout logic, threshold&calibration control, power regulation.

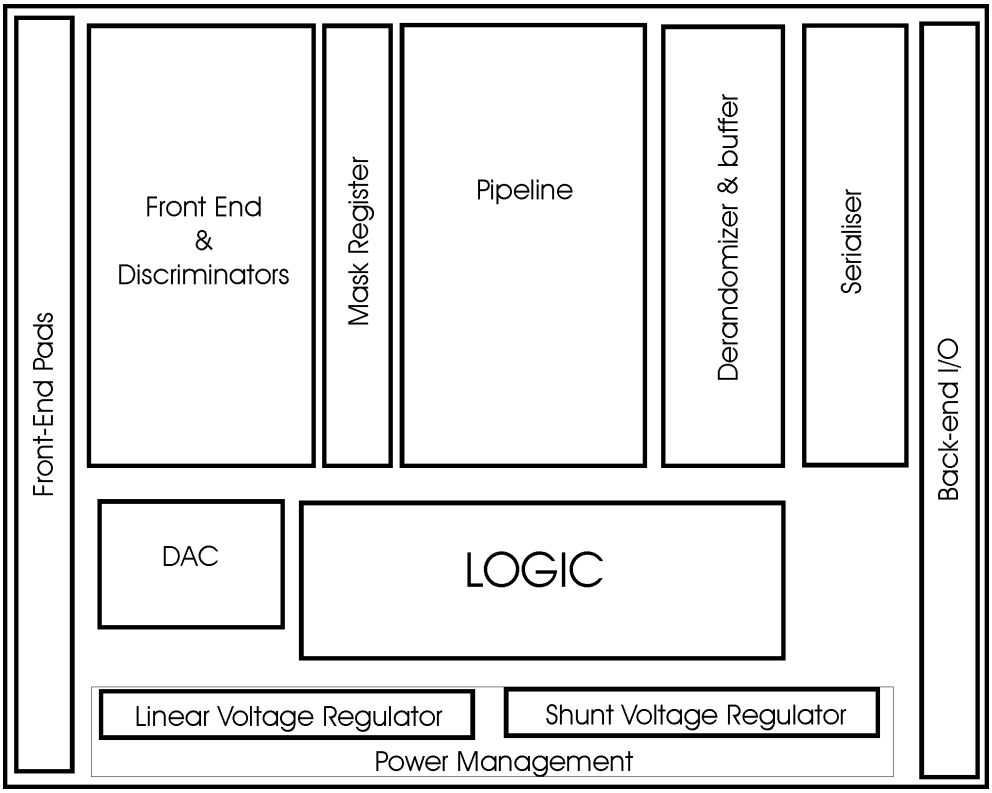

Figure 3-1 Block diagram of the ABC-N chip.

3.1.2 Signal processing

The chip must contain following functions:

1. Charge integration
2. Pulse shaping
3. Amplitude discrimination. The threshold value for the amplitude discrimination is provided as a differential voltage either from internal programmable DAC.
4. The outputs of the discriminators must be latched either in the edge sensing mode or in the level sensing mode.
5. At the start of each clock cycle the chip must sample the outputs from the discriminators and store these values in a pipeline until a decision can be made whether to keep the data.
6. Upon receipt of a L1 Trigger signal the corresponding set of values together with it's neighbours are to be copied into the readout buffer serving as a derandomizing buffer.
7. The data written into the readout buffer is to be compressed before being transmitted off the chip.

8. Transmission of data from the chip will be by means of token passing and is compatible with the ATLAS protocol.
9. The chip is required to provide reporting of some of the errors that occur:
    a) Attempt to read out data from the chip when no data is available.
    b) Readout Buffer Overflow: The readout buffer is full and the chip is not able to keep track of the data held in it. (Chip reset required).
10. The chip shall incorporate features that will enable the system to continue operating in the event of a single chip failure.
11. It is a system requirement that the fraction of data which is lost due to the readout buffer on the chip being full is less than 1%. This assumes that on average only 1% of the silicon strip detectors are hit during any particular beam crossing.

3.1.3 Calibration and testability

Each channel has an internal Calibration Capacitor connected to its input for purposes of simulating a "hit" strip. The Calibration Capacitors are charged by an internal chopper circuit which is triggered by a command. Every fourth channel can be tested simultaneously with group selection determined by two binary coded Calibration Address inputs (CALD0, CALD1). The strobe and the address signals are delivered from the control circuitry. The voltage applied to the Calibration Capacitors by the chopper is determined by an internal DAC. The four calibration bus lines, each of which connects the calibration capacitors of every fourth channel, are also brought out to pads which can be directly driven with an AC coupled voltage step. This is intended for use during IC testing. A tuneable delay of the calibration strobe with respect to the clock phase covering at least two clock periods must be provided. The chip must incorporate such features that will enable to test and calibrate it either on the wafer level or in situ.

3.1.4 Compatibility

The data readout of the ABC-N chip is using the same transmission protocol as the one specified for ABCD. A large degree of compatibility with the existing ATLAS SCT DAQ readout system is therefore maintained. However some changes are described in this document. They are mainly additions to existing features, like the readout of internal registers, which only require additional functionalities in the DAQ system, but do not create incompatibility. If modifications are affecting the existing protocol which was defined for ABCD, then it will be verified that the changes can be implemented in the SCT DAQ system upgrade.

3.2 Specifications

3.2.1 Detector parameters

The design of the ABC-N will be optimised for performance with short strips. The parameters of the short strips pre- and post-radiation, as understood presently, are summarised in Table 3.1.

Table 3-1 : Assumed detector electrical parameters.

	pFZ initial	pFZ $5x10^{14}$	pFZ $9x10^{14}$	pMCZ Initial	pMCZ $5x10^{14}$	pMCZ $9x10^{14}$
Coupling type to amplifier	AC			AC		
Readout strip implant	N			N		
Strip pitch	75.6 µm			75.6 µm		
Coupling capacitance to amp Total for 2.4 cm strips	20 pF/cm 48 pF	20 pF/cm 48 pF	20 pF/cm 48 pF	20 pF/cm 48 pF	20 pF/cm 48 pF	20 pF/cm 48 pF
Capacitance of strip to all neighbour strips	1.3 pF/cm	1.3 pF/cm	1.3 pF/cm	1.3 pF/cm	1.3 pF/cm	1.3 pF/cm
Capacitance of strip to backplane	0.30 pF/cm	0.42 pF/cm	0.48 pF/cm	0.40 pF/cm	0.30 pF/cm	0.33 pF/cm
Extra capacitance in connections, e.g., fan-in	1 pF			1 pF		
Metal strip resistance	15 Ω/cm	15 Ω/cm	15 Ω/cm	15 Ω/cm	15 Ω/cm	15 Ω/cm
Bias Resistor	1.5 MΩ	1.5 MΩ	1.5 MΩ	1.5 MΩ	1.5 MΩ	1.5 MΩ
Max leakage current per strip for shot noise 2.4 cm strips at -15˚C	0.5 nA	0.32 µA	0.6 µA	0.5 nA	0.32 µA	0.6 µA
Charge collection efficiency (at 500 V)	1	0.6	0.45	0.6	0.85	0.6
Collected charge (at 500 V)	24,000	14,000	11,000	14,000	20,000	14,000
Charge collection time	< 10 ns	< 10 ns	< 10 ns	< 10 ns	< 10 ns	< 10 ns

When relevant the specification of the front-end circuits are defined separately for the “initial” detector parameters before irradiation and for the detector parameters “after full dose” of $9x10^{14}$ cm^{-2} n. eq.

3.2.2 Front-end

3.2.2.1 Electrical Requirements:

Note that notation convention for currents used in the entire specification is "+" for current going into (sunk by) the chip and "-" for current going out of (sourced from) the chip.

3.2.2.2 Input Characteristics:

Input Signal Polarity: The front-end circuit can accept input signals of both polarities.

Crosstalk: < 5% (via detector interstrip capacitance, for the interstrip capacitance up to 75% of the total capacitance)

Input Protection: Must sustain voltage step of 500 V of either polarity with a cumulative charge of 0.6 nC in 25 ns.

Open Inputs:	Any signal input can be open without affecting performance of other channels.
Max Parasitic Leakage Current:	200 nA DC per channel with <10% change in gain at 1 fC input charge for nominal bias current in the feedback transistor, can be increased up 375 nA by adjusting the current in expense of some increase of the parallel noise.

3.2.2.3 Preamplifier-Shaper Characteristics

Gain at the discriminator input:	100 mV/fC for the nominal bias currents and the nominal process parameters
Effective gain extracted from the response curve:	90 mV/fC for the nominal bias currents and the nominal process parameters
Linearity:	better than 3% in the range 0 – ±6 fC better than 10% in the range 0 – ±10 fC
Peaking time:	22 ns Intrinsic peaking time of 22 ns of the circuit ensures a peaking time of 25 ns including the effect of charge collection time.
Noise:	Maximum rms noise for nominal components as measured on fully populated modules <= 750 electrons rms for unirradiated module
Gain Sensitivity to analogue supply voltage for 1 fC signal:	1%/100mV

Power Supply Rejection Ratio at:
(not design targets but simulation results of the circuit)

10 Hz - 10 kHz	> 45 dB
10 kHz – 1 MHz	> 10 dB
1 MHz - 12 MHz	> 3 dB
12 MHz - 100 MHz	> -7 dB

3.2.2.4 Comparator Stage:

A threshold is applied as a differential voltage offset to the comparator stage. This threshold voltage is applied from an internal DAC in the normal operation mode (optionally can be applied from external pads for test purposes).

Threshold setting range:	0 fC to ±9 fC, nominal setting at 1 fC before irradiation and 0.5 fC after full dose.	
Threshold setting step without trimming:	0.04 fC (8-bit resolution) of input charge around nominal threshold of 1 fC.	
Threshold spread before trimming	< 4 mV rms (0.05 fC rms)	
TrimDAC resolution	5 bit	
Threshold setting step after trimming	TrimDAC range	TrimDACstep
	0.165 fC (×1)	0.0053 fC
	0.248 fC (×1.5)	0.0080 fC
	0.331 fC (×2)	0.0106 fC
	0.413 fC (×2.5)	0.0133 fC
	0.496 fC (×3)	0.0160 fC
	0.661 fC (×4)	0.0213 fC
	0.827 fC (×5)	0.0267 fC
	0.992 fC (×6)	0.0320 fC

3.2.2.5 Timing Requirements:

Timewalk:	<= 15 ns. This specification depends on the precision of the digital acquisition latch edge. Good alignment, 1 or 2 ns over a common clocked array of channels implies a longer timewalk assignment to the rising edge of the shaped signal.
Timewalk defined:	The maximum time variation in the crossing of the time stamp threshold over a signal range of 1.25 to 10 fC, with the comparator threshold set to 1 fC.
Double Pulse Resolution:	<= 75 ns for a 3.5 fC signal followed by a 3.5 fC signal

Max recovery time for a 3.5 fC signal following a 80 fC signal: 1 μs

3.2.2.6 Threshold Generation Circuit

Differential voltage for the discriminator threshold is generated by two internal DAC circuits (Threshold DAC). The threshold voltages generated by the internal circuits are optionally applied to pads (VTHP and VTHN), to which it is possible to apply external voltages. When the external thresholds are not applied the internal threshold voltages can be measured at pads VTHP and VTHN.

Range:	0 – 816.0 mV
Step value:	3.2 mV
Absolute accuracy:	1%

3.2.2.7 Threshold Correction Circuit

In order to compensate channel-to-channel variation of the discriminator offset each channel is provided with a trim DAC of 5-bit resolution. Each channel can be addressed individually and the threshold correction can be applied channel by channel. The range of the trim DAC can be selected with three bits

in the configuration register (see Table 3-34). This is to cover the offset spread which is expected to increase after irradiation.

Range of the trim DAC: eight selectable ranges

Step value: see Table 3-2

Absolute accuracy: 10%

Table 3-2 : Trim DAC range selection

Trim DAC Code (bit2 bit1 bit0)	**Trim DAC range**	**Trim DAC step**
0 0 0	0 mV – 14.88 mV	0.48 mV
0 0 1	0 mV – 22.32 mV	0.72 mV
0 1 0	0 mV – 29.76 mV	0.96 mV
0 1 1	0 mV – 37.20 mV	1.20 mV
1 0 0	0 mV – 44.64 mV	1.44 mV
1 0 1	0 mV – 59.52 mV	1.92 mV
1 1 0	0 mV – 74.40 mV	2.40 mV
1 1 1	0 mV – 89.28 mV	2.88 mV

3.2.2.8 Calibration Circuit Characteristics

Calibration signal can be applied to one of the four calibration lines via the external pads or from the internal calibration circuit. In the later case the address of the calibration line, the amplitude of the calibration signal and its delay is set via the control logic.

Calibration Capacitors: 50 fF ±8% (3 sigma) over full production skew, ±2% (3 sigma) within one chip.

Calibration signal:

amplitude range: 0 – 204 mV (charge range: 0 – 10.2 fC)

amplitude step: 0.8 mV (charge step: 0.04 fC)

Absolute accuracy of amplitude: 5% (full process skew)

Relative accuracy of amplitude: < 2 % (for known values of calibration capacitors, amplitude range 0.4 to 8 fC, across one chip, including switching pickup, etc.)

Calibration Strobe signal pickup at comparator should be less than 0.05 fC equivalent sensor input.

For test purposes, a voltage step can be applied directly to any one of the four groups of calibration capacitor via the input pads (CAL0, CAL1, CAL2, CAL3). When not used, these four pads must be left floating.

3.2.3 Input Register and Mask Register

The functions of the input register and mask register will be implemented in a single functional block. The input/output connections to this block are shown in Figure 3-2.

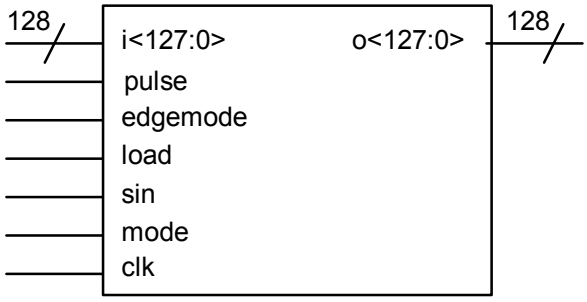

Figure 3-2 Input Register Inputs/Outputs

Table 3-3 : Input Register I/O Signal Definitions

Signal Name	**Active State/Edge**	**Function**
i<127:0>		Hit Inputs (from input translators)
load	Active High	Load Mask Register
sin		Mask/Test Data Input (serial)
mode	see Table 3-5	
clk	Pos Edge	
o<127:0>		Data Outputs (to pipeline)
edgemode	High	Enables edge detection logic
pulse	High	Pulse all outputs simultaneously

3.2.3.1 Input Register

This register latches the incoming data, delivering a well defined pulse width to the pipeline.

3.2.3.2 Edge Detection Circuitry

The function of this block is to detect a low to high transition in the data entering the pipeline, and for each of such transition found the circuit generates a pulse of duration 1 clock cycle irrespective of the length of the incoming pulse. The effect of this block is that only a single '1' is written into the pipeline for every hit detected regardless of the response time of the discriminator. This circuitry can be turned on or off by setting the appropriate bit in the configuration register.

3.2.3.3 Channel Masking Register

This register serves a dual purpose. Firstly, the Channel Mask register enables any bad or noisy channels to be turned off thus preventing them from increasing the data rate due to false hits. Secondly, it can be used during chip testing to apply a set of test patterns to the pipeline. In the test mode the inverted test pattern appears at the output of the pipeline. The contents of this register can be changed by sending the appropriate control command to the chip. A channel is masked with '0'. The test pulse is masked by the mask register as well.

Table 3-4 : Masking Register Modes of Operation

mode	**Mode of Operation**
0	Normal Data Taking (Contents of register used to "Mask Inputs")
1	Test Mode (Contents of mask register are used to supply test values to pipeline)

3.2.4 Pipeline

The binary pipeline is realised by two dual port RAM blocks of 144 bits (wide) by 128 bits (length). The total pipeline length is 256 bits, or 6.7us latency time. Out of the 144 inputs, 128 are for the hit data and 8 are receiving the BC counter data. When a L1 trigger arrives, the hit-pattern and BC count from the three time bins written in the pipeline a predefined number (NUM) clock cycles before are readout and transmitted to the readout buffer. NUM is the number of clock cycles representing the L1 delay time. The value of NUM is programmable through the command decoder and stored in an internal register (L1delay Register). With a command "**reset**" the clock generator is reset while the contents of the pipeline remains unchanged. The input/output connections to the pipeline block are shown in Figure 3-3.

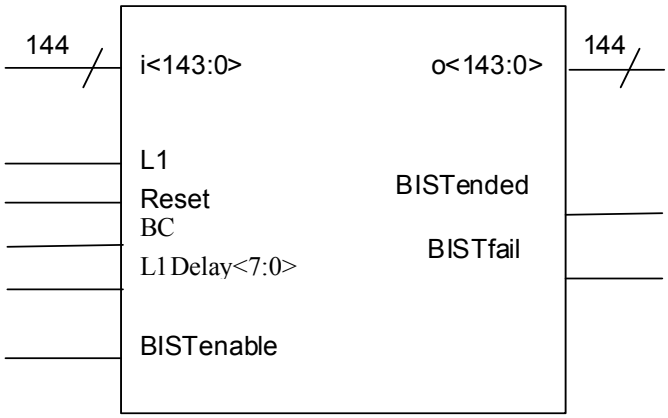

Figure 3-3 Pipeline Input/Outputs.

Table 3-5 : Pipeline Input/Output Signal Definitions.

Signal Name	Active State/Edge	Function
i<143:0>		Data Input
L1	High	Reads Value out of pipeline
Reset	Low	Initialises pipeline pointers and clears accumulator register
BC	Pos edge	Clock input
L1Delay<7:0>		Delay value bits
o<143:0>		Data Output
BISTenable	high	Starts Built-In Self Test
BISTended	high	High when Built-In Self Test in progress
BISTfail	high	Flag high if Built-In Self Test fails

3.2.5 Readout Buffer

Data corresponding to each L1 trigger will be held in a Readout buffer pending readout. This data buffering is needed to remove the statistical fluctuations in the arrival time of L1 triggers. Data compression and read out will be started only when this buffer is not empty (DataAvail =1). Three bits of data will be stored in this buffer for each channel per L1 trigger. These bits represents the three beam crossings centred on the L1 trigger time and are set if the input was above threshold during the corresponding crossings. This buffer will be 180 bits wide by 128 locations deep. This is sufficient to hold the data from 42 L1 triggers. This satisfies in excess the ATLAS specification of maintaining

<= 1% data loss at a L1 trigger rate of 100 kHz and a strip occupancy of up to 1%. The bus width of 180 is used to store the 128 bits from the pipeline, 4 bits of L1 counter, 8 bits of BC counter. The unused bus lines are set to zero.

3.2.5.1 Overflow

Two signals DataAvail and Overflow are produced by the readout buffer. DataAvail indicates when there is data in the buffer to be readout. This signal is used by the Data Compression logic to determine when to start a readout cycle. Overflow indicates when next data entering in the buffer will be overwriting older data and hence data will be lost. Overflow occurs when the buffer contains more than 42 events i.e. 126 samples . This signal is sent to the readout logic which results in the readout logic sending an error message to say that L1 cannot be accepted anymore. This occurs after 42 events are stored in the buffer, which is much more than the expected number of stored events for the worst conditions of occupancy and trigger rate. Should this condition occur, it indicates an abnormal function of the chip or system. The buffer overflow flag can only be cleared by issuing a reset to the chip.

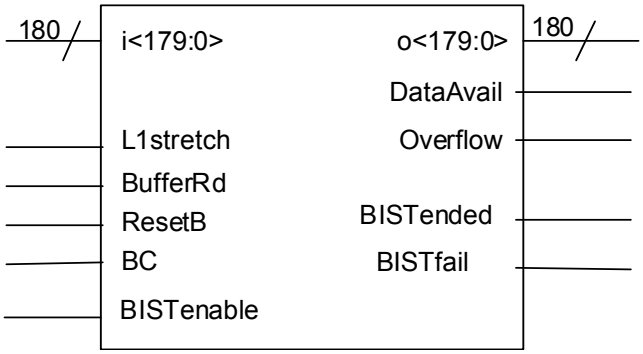

Figure 3-4 Readout Buffer Input/Outputs.

Table 3-6 : Readout Buffer Input/Output Signal Definitions.

Signal Name	Active State/Edge	Function
i<179:0>		Data Input
L1stretch	High	Write value into readout buffer
BufferRd	High	Reads value from readout buffer
ResetB	Low	Resets buffers pointers and counter
BC	Pos edge	Clock input
o<179:0>		Data Output
DataAvail	High	Data available in buffer
Overflow	High	Buffer Overflow
BISTenable	high	Starts Built-In Self Test
BISTended	high	High when Built-In Self Test in progress
BISTfail	high	Flag high if Built-In Self Test fails

3.2.6 Data compression logic

It is anticipated that on any event very few channels will contain hits. This fact can be used to reduce the number of bits of data that have to be read out of the chip for each event. The data compression logic works by examining in turn the 3 bits of data that make up the hit pattern for each channel. Each

group of 3 bits is compared against one of 4 selectable criteria. If the pattern meets the criteria, then the hit pattern from that channel is sent to the readout circuitry for transmission, if not, no data is sent from that channel and the hit pattern from the next channel is examined. This process is repeated until the hit patterns from all 128 channels have been examined. The following table shows the 4 selection criteria (currently there are only plans to use 3, the 4th is for chip testing only).

Table 3-7 : Data Compression Criteria

mode(1:0)	Name of Selection Criteria	Hit Pattern (Oldest data bit 1st)	Usage
00	Hit	1XX or X1X or XX1	Detector alignment
01	Level	X1X	Normal Data Taking
10	Edge	01X	Normal Data Taking
11	Test	XXX	Test Mode

N.B. X = Don't care state.

This block operates as follows.

As soon as the chip receives a L1 trigger, the three 128-bit words that make up an event are written into the read out buffer. This results in the empty flag on the readout buffer being negated, indicating that there is data to be processed. The data compression logic monitors the state of this flag until it finds that there is data available. Providing that it is not already processing data, it then proceeds to read in the three 128-bit words that make up an event from the readout buffer.

The next thing that happens is that the data compression logic re-arranges the order of the data from being 3 128-bit words into 128 3-bit words. The reason for this is that the data compression algorithm requires all 3 samples of an event to be examined in parallel.

The data compression logic then starts to scan through all the channels in turn until it finds one which has a pattern of hits which matches the data selection criteria. If it finds such a pattern of hits, it asserts the "datavalid" signal and places the pattern of hit bits on the "hit<2:0>" outputs and places the address of the hit channel on the address outputs "ch<6:0>". The logic then waits until the readout logic signals it to proceed by asserting the "next" input. The data compression logic responds to "next" by presenting the address and data for the next hit found if any. If the next hit found is on the next adjacent channel, the "adj" is asserted with the data from the previous channel. If no more hits are found, the "end" signal is asserted.

In certain situations, it is not necessary for the data compression logic to process the data from the readout buffer but it is still necessary for it to read the 3 values from the buffer in order to flush them from the readout buffer. There are 3 cases when this happens, these are listed below in order of priority.

1) When the chip is in its SEND_ID mode of operation.

2) When the chip is sending register content (Read register mode)

3) When the Readout Buffer overflow flag has been set.

The following table shows how the datavalid, end and overflowout outputs are used to indicate the status of the data compression logic.

Table 3-8 : Data Compression Logic Output States.

datavalid	end	overflowout	condition
low	low	low	no events available to be read out i.e. readout buffer empty.
high	low	low	data from hit channel waiting to be read out. (not last channel)
high	high	low	data from last hit channel waiting to be read out.
low	high	low	all hits read out or no hits found
low	low	high	data for event lost due to readout buffer overflow

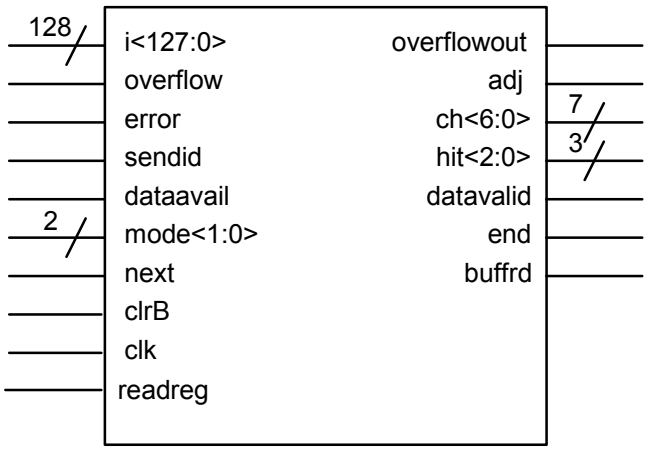

Figure 3-5 Data Compression Logic Input/Outputs.

Table 3-9 : Data Compression Logic Input/Output Signal Definitions

Signal Name	Input/Output	Active State/Edge	Function
i<127:0>	input		Data Input
overflow	input		Overflow output from readout buffer
error	input		Error output from readout buffer
sendid	input		indicates sendid mode of operation
readreg	input		indicates register read mode of operation
dataavail	input	High	Data available to be readout
mode<1:0>	input		Selects data compression mode
next	input	High	Find next hit channel.
clrB	input	Low	Resets logic
clk	input	Pos Edge	Clock Input
overflowout	output	High	Overflow output to readout circuitry
adj	output	High	Next Hit found on adjacent channel
ch<6:0>	output		Channel address of Hits
hit<2:0>	output		Hit Data pattern
datavalid	output	High	Hit Data outputs valid
end	output	High	Last Channel scanned
buffrd	output	High	Reads Value out of Readout Buffer

3.2.7 Readout Circuitry

The readout circuitry will be responsible for capture and release of the token and outputting data from the chip. The readout circuit always waits until the token arrives. On arrival of the token, it checks if any hits have been found by the data compression logic. If so, it then outputs the appropriate header information. It then proceeds to output the address of the hit channel together with the data from that channel. Once the readout circuitry has finished sending the data from one channel, it proceeds to output the data from then next channel. In the situation where one or more neighbouring channels are to be read out, only the address of the first channel is sent, but the data from all hit channels are sent. This process continues until the data compression logic indicates that all channels have been examined by asserting "end". Once all the data corresponding to a single event has been read out, a token is sent out to the next chip in the readout chain. This token will be sent out ahead of the last bit of data sent out. If the chip has no data to be readout, circuitry sends out a "No hit data" code and passes the token on to the next chip in the chain.

If the chip is in "send-id" mode, or in reading register mode, or the readout buffer has overflowed or generated an error condition, the readout circuitry sends the appropriate error packet or register data packet. In these cases the readout circuitry is still required to signal to the data compression logic that it has processed an event by asserting the "next" signal. This operation is needed so that a correct count of the number of events waiting to be read out can be maintained.

In the case of an error condition occurring, e.g. attempt to readout data and no data available, the appropriate error code will be sent by the readout logic. If the chip is in the "send_id" mode of operation, no data or error codes are output from the chip but instead a special packet of data containing information about the chips current configuration is sent.

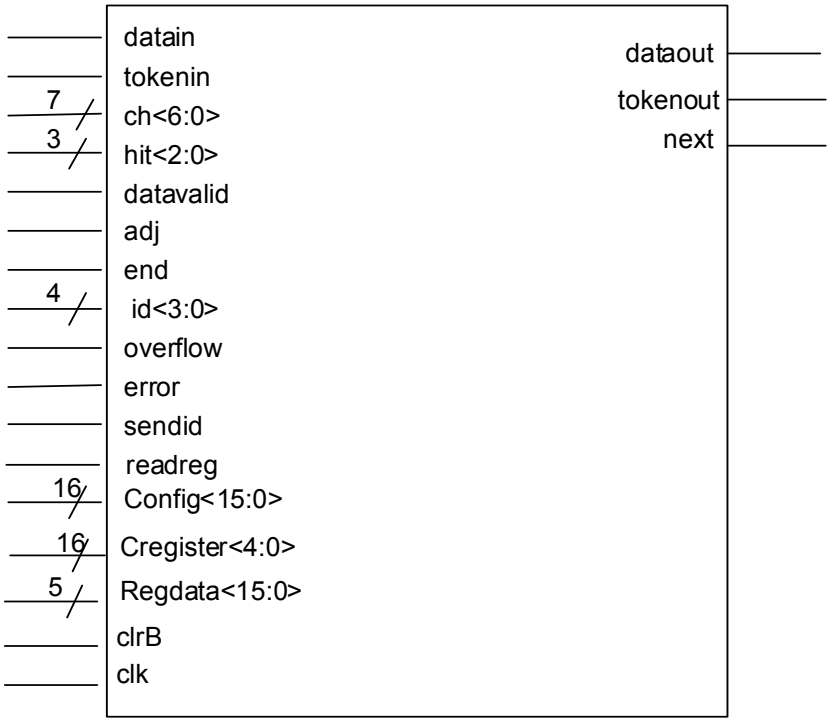

Figure 3-6 Connections to Readout Circuitry

Table 3-10 : Readout Logic Input/Output Signal Definitions

Signal Name	Input/Output	Active State/Edge	Function
datain	input		Data Input
tokenin	input	High	Token Input
ch<6:0>	input		Address of Hit Channel
hit<2:0>	input		Hit data pattern
datavalid	input	High	Data available for sending
adj	input	High	Hit found on adjacent channel
end	input	High	End of data to be sent
id<6:0>	input		Chip address
overflow	input	High	Readout buffer Overflow
error	input	High	Readout Buffer Error
sendid	input		Chip mode of operation
readreg	input		Chip mode of operation
config<15:0>	input		Data from config-reg
regdata<15:0>	input		Data from Read Register
Cregister<4:0>	input		Address of Read Register
clrB	input	Low	Resets circuit
clk	input	Pos Edge	Clock input
dataout	output		Data output
tokenout	output		Token Output
next	output	High	Scan Next Channel

3.2.8 Readout Controller Block

This block is to control the readout of data from several ABC-N chips connected together in a token chain.

The ABC-N chip can be configured as “Master” (Master bit set, bit 11 of CFG1 register) or as “End” (End bit set, bit 12 of CFG1 register). If none of these bits are set, the chip is in “Slave” configuration.

There are two ways to initiate a readout sequence:

1. The readout is enabled by placing the chip in "Master Mode" and it receives a L1 trigger. In this mode, the chip readout sequence starts immediately after the readout buffer is not empty (ie at least one L1 trigger has been received). At the end of its own data readout sequence, the chip issues a token to the next ABC-N chip connected to it, collects the data from this neighbour chip and then from all other adjacent chips which receive successively the token and backward data in response. The readout sequence is terminated when the Master chip receives a trailer pattern (described in 3.2.28) in which case the readout sequencer resumes and the chip is ready to restart a sequence as long as the readout buffer is not empty. With this mode, the data is serially transmitted through the Large Drive Outputs (Ldo, LdoB) of the chip.
2. The readout is enabled by placing the chip in “Slave Mode” (ie not Master) or “End” Mode, and receives a token. In this mode, the chip readout sequence starts immediately after the token has been received. At the end of its own data readout sequence, the chip issues a token to the next ABC-N chip connected to it, collects the data from this neighbour chip and then

from all other adjacent chips which receive successively the token and backward data in response. With this mode, the data is serially transmitted through the Data Output lines (DataOut, DataOutB) of the chip.

For the chip in Master mode the readout sequence starts with a preamble, then L1 and BC counters values are transmitted before the other data is sent. The chips in Slave or End mode do not transmit the counters content. The chip in "End" mode adds a specific pattern (trailer) to its data packet (see 3.2.28).

3.2.8.1 L1 Counter

This a 4-bit binary counter which is incremented every time the chip receives a L1 trigger. The counter is zeroed by either a hardware reset or a software reset. The L1 counter value is entered in the readout buffer at the time of a L1 signal receipt.

3.2.8.2 Beam Crossing Counter

This is an 8-bit binary counter which is incremented on every clock cycle. This counter is zeroed by either hardware reset, a software reset, or a special BC Reset Command. The BC counter value is entered in the pipeline at each clock cycle and transferred to the readout buffer at the time of a L1 signal receipt.

3.2.8.3 Token Generation Logic

The purpose of the token generation logic is to detect when the chip set in "Master" mode has received an L1 trigger and to generate a token to initiate the read out of data from that L1 trigger. This logic waits until the readout buffer becomes not empty and it then issues a token. It then monitors the data passing through it from all the chips in the chain looking for a "Trailer" bit pattern. It waits until this trailer is detected before checking to see if the readout buffer is empty. If the readout buffer is still not empty it repeats the cycle.

3.2.8.4 Data Formatting Logic

The purpose of this logic is to attach the header or trailer patterns to the packets of data of the chip set in "Master" or "End" mode. The header information contains a preamble and the L1 and BC counters values, which are sent prior to the data of the chip set in "Master" mode. This logic attaches the "trailer" bit pattern to the packet of data of the chip set in "End" mode.

3.2.8.5 Serial Data Output Driver (ldo)

This is the output from the chip set in "Master" mode to send data to the local module controller or to the DAQ system. The formatted data, and the token generation circuitry, are clocked from the separate clock input "Clk". This clock receives the serialisation clock signal which can be as high as 160MHz. This clock has to be synchronous with the main clock source for the chip (BC clock, 40MHz).

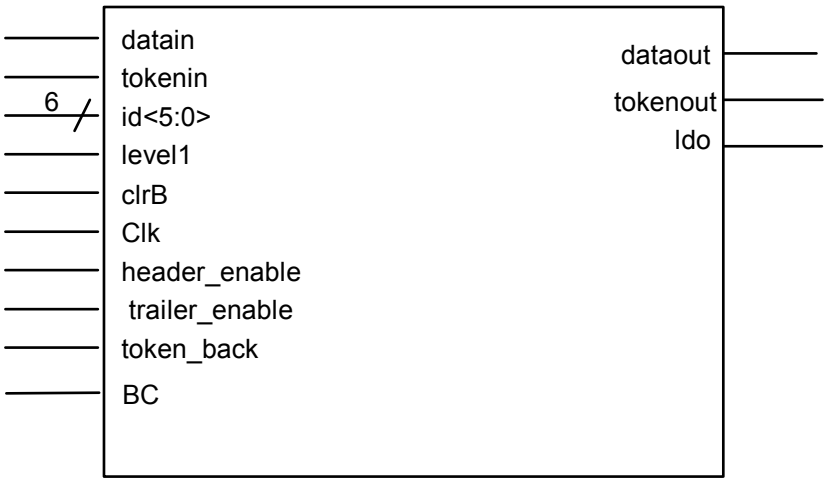

Figure 3-7 Connections to Readout Controller Circuitry.

Table 3-11 : Readout Controller Input/Output Signal Definitions

Signal Name	Active State/Edge	Function
datain		Serial Data Input
tokenin	High	Token Input
id<6:0>		Address of chip
level1	High	L1 Trigger
clrB	Low	Resets block
BC	Pos Edge	Clock input
Clk		Clock for Serial data out to LED driver
dataout		Serial data output
tokenout	High	Token Output
header_enable	High	Enables Generation of Packet Header
trailer_enable	High	Enables Generation of Packet Trailer
token_back	High	Input for Token output from ROL
ldo		Serial data out in Master mode

3.2.9 Serial Data Output Readout Modes

3.2.9.1 Stand-alone mode

This mode is used when ABC-N chips are grouped and one ABC-N is configured as “Master”, another one as “End”. When receiving L1, the “Master” chip sends a preamble, its own data, and a token to adjacent chip. This token is passed from chip to chip in the group up to the one in “End” mode, which emits a specific pattern to mark the end of the readout. Data from the group are passed successively through the “Master” chip which transmits to the next readout level.

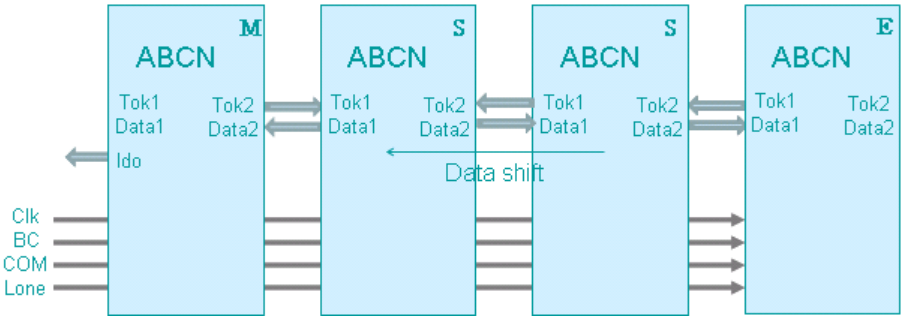

Figure 3-8 ABC_N readout connexions in stand-alone mode.

3.2.9.2 Module Controller mode

This mode is used when ABC-N chips are grouped and the data are collected by a local controller chip (MC). In this mode all the chips but one are in “slave” mode, and one is set in “End” mode. The controller chip emits a token to the first ABC-N chip. This token is passed from chip to chip in the group up to the one in “End” mode, which emits a specific pattern to mark the end of the readout. Data from the ABC-N group are passed successively to the controller.

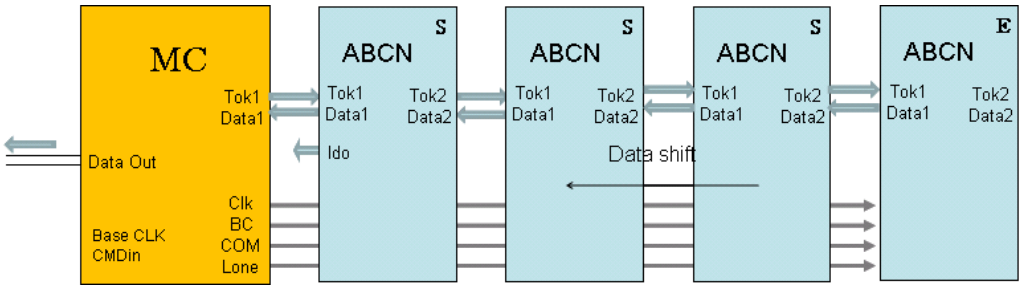

Figure 3-9 ABC_N readout connexions with a module contoller

3.2.10 Command Decoder

The command and control information all comes into the chip on the command input pins. There are two main classes of information which arrive here, L1 Triggers Commands and Control Commands. These are distinguished by a 3-bit code. Furthermore two types of Control Commands are possible, Fast Control Commands and Slow Control Commands. Depending on which class arrives, further information may follow. This further information will also need decoding, formatting and sending to the appropriate functional blocks of the chip. More detailed information is contained in 3.2.18 and the actual data fields of the commands are listed in Table 3-43 and Table 3-44. The two classes of Commands and two types of Control Commands are:

3.2.10.1 L1 Trigger Command

If the 3-bit code indicating this command is received by the Command Decoder, or if an external L1 signal is received ("Lone" inputs), the control logic writes 3 samples from the pipeline or the accumulator register, into the Readout Buffer. One bit in the L1Delay register can be set to disable the external Lone inputs.

3.2.10.2 Control Commands

If the 3-bit code indicating a Control Command is received, the second field of 4 bits is decoded to determine if it is a Fast Control Command or a Slow Control Command. If a Fast Control Command is decoded, the appropriate command is executed. No address or data fields are included in these commands..

3.2.10.3 Slow Control Command

If the second field of the command is decoded to be a Slow Control Command, the third, forth, fifth and possibly sixth field is decoded to determine the full action required. These Slow Control Commands are of variable length and the contents of the third field determines the total number of bits to be processed.

The command decoder block is required to decode the command and send the relevant instruction and data to other parts of the chip. The input/output connections of the Command Decoder are shown in Table 3-12.

Table 3-12 : Command Decoder Input/Output Signal Definitions

Signal Name	Dir	Active State/Edge	Function
id<5:0>	I		Chip ID
command	I		Command Data Input
clrB	I	Low	Reset Input
clk	I	Pos Edge	Clock Input
L1	O	High	L1 signal
SoftReset	O	High	Software controlled reset
BCR	O	High	Beam crossing reset

DTmode	O	High	Sets chip in data taking of operation
REGmode	O	High	Sets chip read register mode of operation
CalPulse	O	High	Send Calibration pulse
TestPulse	O	High	Send Test pulse
TestMaskCLK	O	High	Mask Register Clock (serial loading)
TestMaskIN	O	High	Mask Register Input (serial input)
CalDelayCLK	O	High	Calibration delay register Clock (serial loading)
CalDelayIN	O	High	Calibration delay register input (serial input)
TrimsCLK	O	High	TrimDAC register Clock (serial loading)
TrimsIN	O	High	TrimDAC register input (serial input)
Config1Load	O	High	Loads Configuration Register 1
Config2Load	O	High	Loads Configuration Register 2
Thresh1Load	O	High	Load Threshold Register
Bias1Load	O	High	Load Bias Register 1
Bias2Load	O	High	Load Bias Register 2
Bias3Load	O	High	Load Bias Register 3
L1DelayLoad	O	High	Load Trigger Latency Register
CalRegLoad	O	High	Load Power Control register
CalDelayOUT	I	High	Calibration Delay Register output
Config1OUT	I	High	Configuration Register 1 output
Config2OUT	I	High	Configuration Register 2 output
Thresh1OUT	I	High	Threshold Register output
Bias1OUT	I	High	Bias Register 1 output
Bias2OUT	I	High	Bias Register 2 output
Bias3OUT	I	High	Bias Register 3 output
L1DelayOUT	I	High	Trigger Latency Register output
CalRegOUT	I	High	Calibration Amplitude Register output
StatusRegister1OUT	I	High	Status Register 1 output
StatusRegister2OUT	I	High	Status Register 2 output
MirrorRegister	O	High	Readout Register (for Readout Logic)
Cregister	O	High	Read Register Address

3.2.11 Registers

The Command Decoder controls eight serial access registers with a cached register, three serial access registers with no cache, two status read-only registers and two registers used for the readback function. The registers list and type are listed in Table 3-13.

Table 3-13 : List of registers in ABC-N chip

Register Name	Length	Type	Function
CFG1	16	Cached	Configuration (as in ABCD)
CFG2	16	Cached	IO drive
ThreshReg	16	Cached	Main Threshold
BiasReg1	16	Cached	FECurrent Bias
BiasReg2	16	Cached	FECurrent Bias
BiasReg3	16	Cached	FECurrent Bias
L1DelayReg	16	Cached	L1 Latency setting
CalReg	16	Cached	Calibration amplitude
STAT1	16	Readout only	Status Read register
STAT2	16	Readout only	Status Read register
Test/Mask	128	Serial	Test/Mask Register
CalDelay	16	Serial	Cal pulse delay
TrimsReg	16	Serial	Trims DAC register
Mirror Register	16	Parallel	Data register for readback
Cregister	6	Parallel	Address register for readback

3.2.11.1 Cached Register

The registers of type “Cache” are all 16 bits wide and are used to hold the SEU sensitive information in ABC-N. The following figure and table define the inputs and outputs in this register type.

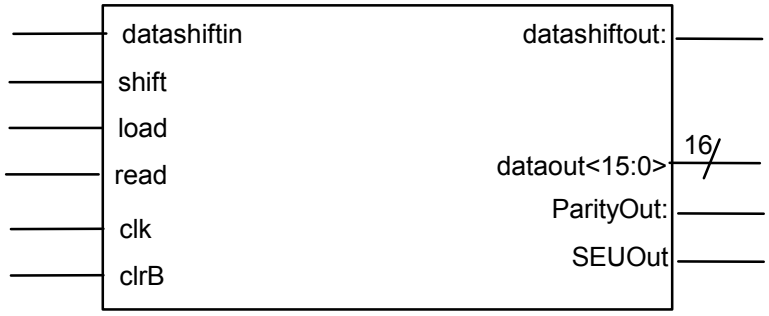

Figure 3-10 Cached register Inputs/Outputs.

Table 3-14 : Cached Register Input/Output Signal Definitions

Signal Name	**Active State/Edge**	**Function**
shift	High	Data input Enable
datashiftin		Data serial input
load	Pos Edge	Transfers data to cached register
read	Pos Edge	Transfers data from cached register
clrB	Low	Resets register to default values
dataout<15:0>		Data Outputs See section 3.2.5
datashift out		Serial data output (read function)
ParityOut		Parity Bit
SEUOut	High	SEU bit

This type of register is made of one serial access register, which receives serialized data from the Command Decoder (the data field of Command Protocol), or sends serial bits representing the content of the cached register for the readout function. The cached register is a parallel-in parallel-out triple vote logic register with auto correction, which is loaded by the data received by the serial register. The outputs of the cache register are readable through the serial access register with the "read" signal.
The ParityOut is the data content parity bit which is used by the Command Decoder and it can be read through the STATUS Registers. The SEUOut is set to one if a SEU has been detected by the auto-corrected cache register. It is read through the STATUS Registers. It is cleared by a software reset.

3.2.11.2 Serial Register

The registers of type "serial" are serially accessed for loading or reading. The following table indicated which function is implemented for each register of this type.

Table 3-15 : Serial registers implemented functions

Register Name	Length (N)	Function
Test/Mask	128	Serial load only
CalDelay	16	Serial load and serial read
TrimsReg	16	Serial load and serial read

The register inputs and outputs definitions are given in Figure 3-11 and Table 3-16.

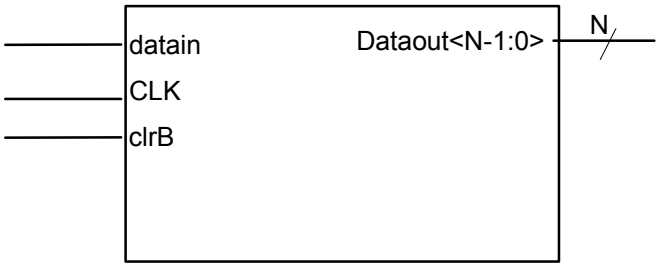

Figure 3-11 Strobe Delay Register Inputs/Outputs.

Table 3-16 : Serial Register Input/Output Signal Definitions

Signal Name	Active State/Edge	Function
datain		Serial data input (command data field)
CLK	Edge	Clock enabled with data
clrB	Low	Resets register
Dataout		Register outputs. DataOut<N-1> is the serial data output for read back function if used.

3.2.11.3 Status Registers

The status registers are made of collection of read-only latches or flip-flops which are attached to logical functions. The logical states are collected at the time the status register read command is issued. A software reset command clears all the bits of the status registers.

3.2.11.4 Command Decoder Registers

When a read register command is issued, the two registers named MirrorRegister and Cregister are loaded with the register data to be read and the corresponding register address. The MirrorRegister is receiving its data from any of the readable register described in 3.2.11. The data is serially loaded except for the two read-only STATUS registers data which are received in parallel. The Cregister is loaded with the address of the register which is being read.

3.2.11.5 Configuration Register 1 (CFG1)

This is a 16-bit register which is used to hold information about the chip's current configuration. The following table defines the usage of the bits in this register and its default value at power-up. The content of this register is not affected by a software reset command.

Table 3-17 : CFG1 Configuration Register Contents

Bit	Name	Function
0-1	Readout Mode*	Selects the data compression Criteria (see Table 3-7)
2-3	Cal_Mode<1:0>	Selects the Calibration code (see Table 3-40). The state of these two bits also determines which channels are tested when Test Mode is enabled.
4-6	Trim DAC range <2:0>	Selects the range of the trim DAC
7	Edge_Detect*	When this bit is Set the edge detection circuitry in the input stage is enabled.
8	Mask *	When this bit is set the input register is disabled and the contents of the mask register are routed into the L1 pipeline.
9	Flow Direction	This bit determines token/data flow direction
10	not used	
11	Master **	When clear the chip acts as a Master providing the masterB input pin has be asserted
12	End*	When set this bit configures the chip as the end of a readout chain.
13	Feed_Through	When clear the chip outputs a 20MHz clock signal but only is the chip has been configured as a Master (see above)
14-15	ThDacOffset<1:0>	Threshold DACs offset setting
SR	SofReset	No effect
HR	HardReset	$0000

* This bit is "ored" with the value on the "masterB" input. If the result is "0", the chip is placed into master mode. Otherwise, it is placed into slave mode (bit12 cleared) or End mode (Bit12 set).

3.2.11.6 Configuration Register 2 (CFG2)

This is a 16-bit register which is used to hold information about the chip's current configuration. The following table defines the usage of the bits in this register and its default value at power-up. The content of this register is not affected by a software reset command.

Table 3-18 : CFG2 Configuration Register Contents

Bit	Name	Function
0-4	DriveUp	Drive current of top side token/data drivers
5-9	DriveBot	Drive current of bottom side token/data drivers
10		
11		
12		
13		
14		
15		
SR	SofReset	No effect
HR	HardReset	$0000

3.2.11.7 Calibration Register (CalReg)

The Calibration register holds the calibration pulse amplitude value. The outputs of this register are used to control 8-bit current DAC. The DC current level is used in the calibration circuit to generate calibration signals. This register is not affected by software reset. The power up value of this register will be $0000 (all bits at zero).

Table 3-19 : CalReg Register Contents

Bit	Name	Function
0-7	CalPulse	8 bits Calibration pulse amplitude, bit 7 is MSB
8-15	Reserved	Shunt regulator adjustement
SR	SoftReset	No effect
HR	HardReset	$0000

Table 3-20 : Calibration DACs - range and resolution

	Range	Resolution
Calibration signal amplitude	0 - 204 mV	0.8 mV/step
Calibration charge injected via 100 fF cap	0 – 10.2 fC	0.04 fC/step

The reference current for the calibration DAC is generated internally in the chip. This reference current will be scaled at the output of the DAC by a value of 0 to 255 depending on the setting of the Calibration register.

3.2.11.8 Threshold Register (ThresReg)

The Threshold register holds the values of two discrimination thresholds. The effective discrimination threshold is set by two independend 8-bit DACs. Depending on the polarity of input signal one of the two DACs is set to 0 and the other is set at a value corresponding to the required threshold. One

threshold value is held in the MS byte of this register and the other one is held in the LS byte of this register. The outputs from these DACs supply 2 independent DC current levels to the threshold generation circuit. This register is not affected by software reset . The power up value of this register will be $00FF (MS byte at zero, LS byte at one).

Table 3-21 : ThresReg Register Contents

Bit	Name	Function
0-7	Threshold VTHP	8 bits Positive threshold level , bit 7 is MSB
8-15	Threshold VTHN	8 bits Negative threshold level , bit 15 is MSB
SR	SoftReset	No effect
HR	HardReset	$00FF

The reference current for the two threshold DACs is generated internally in the chip. This reference current will be scaled at the output of each DAC by a value of 0 to 255 depending on the setting of the Threshold register.

Table 3-22 : Threshold DACs - range and resolution

	Range	Resolution
Threshold voltage	0 - 816 mV	3.2 mV/step

3.2.11.9 Bias Register 1 (BiasReg1)

The 16 bits Bias register 1 holds binary values for 3 5-bit DACs, setting current values of the input transistor, preamplifier feedback and preamplifier buffer. This register is not affected by software reset. The power up value of this register will be $0000 (all bits at zero).

Table 3-23 : Bias1 Register Contents

Bit	Name	Function
0-4	Ipre	5 bits DAC value for preamplifier bias Bit 4 is MSB
5-9	Ipreb	5 bits DAC value for preamplifier buffer bias Bit 9 is MSB
10-14	Ipref	5 bits DAC value for preamplifier feedback bias Bit 14 is MSB
15	not used	
SR	SoftReset	No effect
HR	HardReset	$0000

Table 3-24 : Bias DACs - range and resolution

	Range	Resolution
Ipre Input transistor bias current	27 – 66 μA	1.26 μA/step
Ipreb Preamplifier feedback bias current	1.8 – 11 μA	0.30 μA/step
Ipref Preamplifier buffer bias current	5.4 – 13.2 μA	0.25 μA/step

3.2.11.10Bias Register 2 (BiasReg2)

The 16 bits Bias register 2 holds binary values for 2 5-bit DACs, setting current values of the shaper and shaper feedback circuits. This register is not affected by software reset. The power up value of this register will be $0000 (all bits at zero).

Table 3-25 : Bias Register 2 Contents

Bit	Name	Function
0-4	Ish	5 bits DAC value for shaper bias Bit 4 is MSB
5-9	Ishb	5 bits DAC value for shaper buffer bias Bit 9 is MSB
10-15	not used	
SR	SoftReset	No effect
HR	HardReset	$0000

Table 3-26 : Bias DACs - range and resolution

	Range	Resolution
Ish Shaper bias current	5.4 – 13.2 μA	0.25 μA/step
Ishf Shaper feedback bias current	6.3 – 13.2 μA	0.22 μA/step

3.2.11.11Bias Register 3 (BiasReg3)

The 16 bits Bias register 3 holds binary values for 2 5-bit DACs, setting current values of the differential stage and of the comparator circuits. This register is not affected by software reset. The power up value of this register will be $0000 (all bits at zero).

Table 3-27 : Bias Register 3 Contents

Bit	Name	Function
0-4	Idif	5 bits DAC value for preamplifier bias Bit 4 is MSB
5-9	Icom	5 bits DAC value for preamplifier buffer bias Bit 9 is MSB
10-15	not used	
SR	SoftReset	No effect
HR	HardReset	$0000

Table 3-28 : Bias DACs - range and resolution

	Range	Resolution
Idif Differential stage bias current	18 – 44 μA	0.84 μA/step
Icom Comparator bias curent	18 – 44 μA	0.84 μA/step

3.2.11.12L1 Delay Register (DelayReg)

This is a 16-bit register which is used to hold information about the L1 trigger latency value. The following table defines the usage of the bits in this register. The power up value of latency value will be 255. The contents of this register is not affected by a software reset command.

Table 3-29 : L1 Delay Register Contents

Bit	Name	Function
0-7	L1 Delay	BC clock number representing the L1 delay (binary code, MSB = Bit 7)
8		not used
9	L1mode 0	L1 from Command only
10		not used
11		not used
12		not used
13		not used
14	P_BIST Enable	Pipeline Built_In Self Test Enable
15	D_BIST Enable	Derandomizer Built_In Self Test Enable
SR	SoftReset	No effect
HR	HardReset	$00FF

3.2.11.13Status Register 1 (STAT1)

This is a 16-bit register which is used to hold information about the chip's status and configuration. This is a read-only register. The following table defines the usage of the bits in this register. The content of this register is the direct image of internal signals and is not affected by either Reset.

Table 3-30 : Status Register 1 Contents

Bit	Name	Function
0	BISTended*	Pipeline BIST Ended
1	DeraBISTended*	Derandomizer BIST Ended
2	SCUnusedCode*	False slow command CD code detected
3	FCUnusedCode*	False Fast command CD code detected
4	Clock Rate 0	Clock rate setting, bit0
5	Clock Rate 1	Clock rate setting, bit1
6	Master*	Master enabled
7	End*	End enabled
8	Shuntmode	Shunt enabled
9	VRegmode	Voltage Regulator enabled
10	L1mode 0	L1 detection type (command only)
11	Not used	not used. Read as zero

12	DataAvail*	Derandomizer not Empty
13	Overflow*	Derandomizer Overflow
14	P_BIST_error*	Pipeline BIST Test output
15	D_BIST_error*	Derandomizer BIST Test output
SR	SoftReset	No effect
HR	HardReset	No effect

3.2.11.14Status Register 2 (STAT2)

This is a 16-bit register which is used to hold information about the chip's status and configuration. This is a read-only register. The following table defines the usage of the bits in this register. The power up value of this register will be zero. The contents of this register are cleared by a software reset command.

Table 3-31 : Status Register 2 Contents

Bit	**Name**	**Function**
0	L1SEU*	L1 counter SEU detected
1	BCSEU*	BC counter SEU detected
2	CFG1_SEU	CFG1 register SEU detected
3	CFG2_SEU	CFG2 register SEU detected
4	CALA_SEU	Calibration Amplitude SEU detected
5	TH_SEU	Threshold register SEU detected
6	BIAS1_SEU	Bias1 register SEU detected
7	BIAS2_SEU	Bias2 register SEU detected
8	BIAS3_SEU	Bias3 register SEU detected
9	Delay_SEU	Delay register SEU detected
12	Parity	Parity bit Error detected when reading register
13	TBD	X SEU detected
14	TBD	Y SEU detected
15	SEU*	Any detected SEU occurrence
SR	SoftReset	$0000
HR	HardReset	$0000

3.2.11.15Calibration Pulse Delay Register (CalDelay)

The Calibration Delay Register is a 16 bit register on which only the least significant 8 bits are used. The value stored in this register determines the relative delay between the rising edge of the Calibration Pulse output and the rising edge of the clock input. This delay can be set in 64 steps, of approximately 0.8ns ±0.2ns each, enabling the delay of Calibration Pulse to be swept thought at complete clock cycle at 40MHz. Data is shifted into the register with the MS bit first.

Table 3-32 : Calibration Pulse Delay Register Contents

Bit	Name	Function
0-5	CalDelay	6 bits value for Calibration Pulse delay selection
6-7	Step	2 bits value for selection of Step of the delay
8-15	not used	
SR	SoftReset	No effect
HR	HardReset	$0000

The value of delay is determined according to the following formula.

delay = min_delay + (CalDelay_value x Step_value)

Where :

min_delay is the delay produced when the register is set to zero .

CalDelay_value is the value written into the delay register (least significant 6 bits only)

Step_value is the increase in delay produced by incrementing the contents of the delay register

Table 3-33 : Strobe delay - range and resolution

StepCode (bit7 bit6)	DelayRange	DelayStep
00	0 ns	0 ns
01	50.4 ns	0.8 ns
10	63.0 ns	1.0 ns
11	81.9 ns	1.3 ns

The DelayStep values may vary by +/-20% with process parameters from lot to lot.

3.2.11.16Trim DAC Register (TrimReg)

The TrimDac register holds the address of a channel and a threshold correction value for the given channel. Bits 4:0 of the register are used to set the DAC which controls the offset of the comparator for the given channel. Bits 11:5 are used to set address of the channel .

Table 3-34 : Trim DAC Register Contents

Bit	Name	Function
0-4	Trimdata	5 bits value for DAC threshold correction value Bit 4 is MSB
5-11	Trimadd	7 bits channel address Bit 11 is MSB
12-15	not used	
SR	SoftReset	No effect
HR	HardReset	$0000

3.2.12 Clock and Command Inputs

3.2.12.1 Clock and Command

Two sets of clocks, L1 and command inputs will be provided in order to make the system in which the chips will be used fault tolerant and to provide an additional method of setting up the timing of the system. Each chip will be supplied with two independent sources of clocks, L1 and commands. In the event of the fall out of one of these sources, the alternative source can be used. An external input to the chip "select" will be used to determine which pair of inputs will be used by the chip.

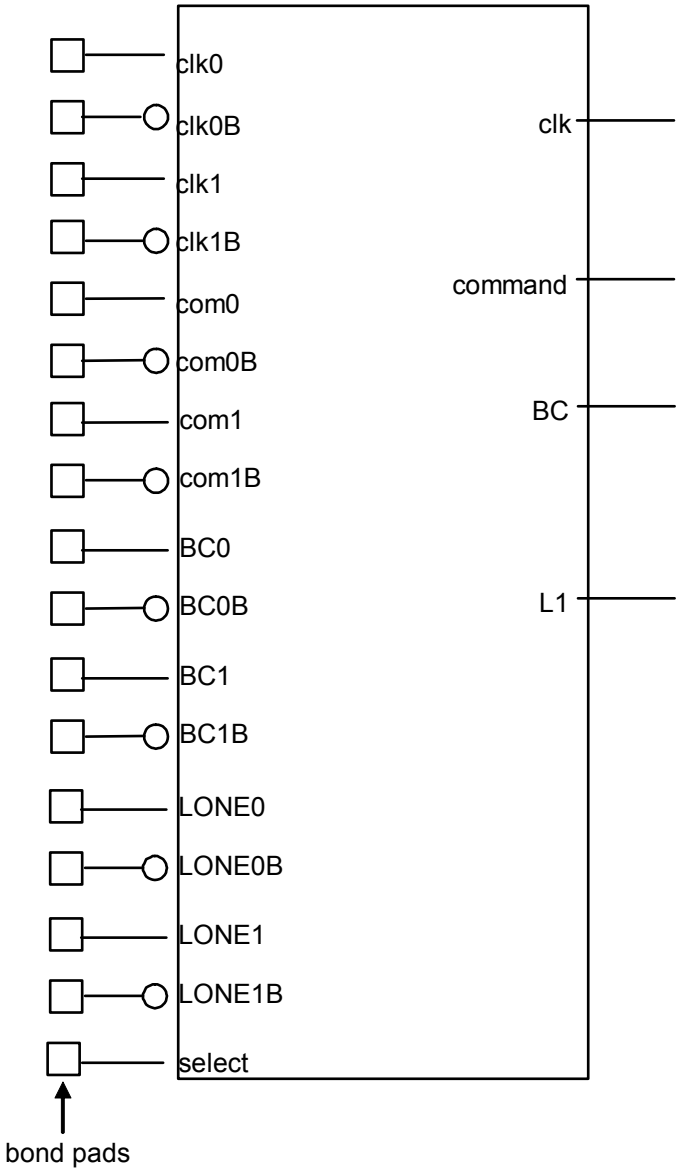

Figure 3-12 Clock & Command Data Inputs.

Table 3-35 : Clock Input/Output Signal Definitions

Signal Name	Active State/Edge	Function
clk0		default Serializer Clock Input
clk0B		Complement of above
clk1		reserve Serializer Clock Input
clk1B		Complement of above
com0		default Command Input
com0B		Complement of above
com1		reserve Command Input
com1B		Complement of above
BC0		default Bunch Crossing Clock Input
BC0B		Complement of above
BC1		reserve Bunch Crossing Clock Input
BC1B		Complement of above
LONE0		Default external L1 Input
LONE0B		Complement of above
LONE1		reserve external L1 Input
LONE1B		Complement of above
clk		Serializer Clock output
command		Command Output
BC		BC Clock Output
LONE		External L1 Output

Table 3-36 : Clock Input Modes of Operation

select	clk	command	BC	LONE
Low	clk0	com0	BC0	LONE0
High	clk1	com1	BC1	LONE1

3.2.12.2 Readout at 40, 80 or 160MHz Clock

The chip receives two clock inputs, one (BC) at 40MHz in synchronization with the beam crossing rate, another one (Clk) which can run at different clock rates, either 40MHz, 80MHz or 160MHz. The Clk rate is the one used for the data serialization. It has to be synchronous with the main beam crossing rate (BC).
Two control bits Clkmode160 and Clkmode80, driven by external pads, are reserved for configuring the chip operation according to the Clk clock rate.

Table 3-37 : Clock Rate Settings

ClkMode80	ClkMode160	Applied clock rate
0	0	40MHz
1	0	80MHz
0	1	160MHz
1	1	40MHz

3.2.13 Chip ID

The chip address field is expanded to 7 bits, different from the ABCD case, where it was 6 bits (and only 4 bits transmitted). It has an implication on the system level as the command protocol and the data readout protocol have to be modified consequently.

To enable a chip to be individually addressed seven inputs ID(6:0) will be used to implement a geographical addressing scheme. This is because there may be up to a total of 40 chips on each module side, and under certain conditions it may be necessary to address all the chips on 2 module sides. These inputs will be wire bonded to a unique set of logic levels on each chip mounted on the detector module. This set of logic levels will form a geographical address which will enable individual chips on the module to be addressed. Each address input has an internal pull-up. The address "1111111" (127) is reserved for global addressing (all chips respond).

3.2.14 Token and Data Input/Output Circuits

In order to provide some measure of fault tolerance in the system, the token and data signals are bidirectional : the purpose of this is to enable a chip to receive or send it's token and data from/to it's two direct neighbours. Each chip has then 2 bidirectional token ports and 2 bidirectional data ports. In this way, should one of chip's neighbours fail, the other chip's neighbour can replace it. One bit set in the CFG1 register is used to direct each chip to one neighbour or the other one.

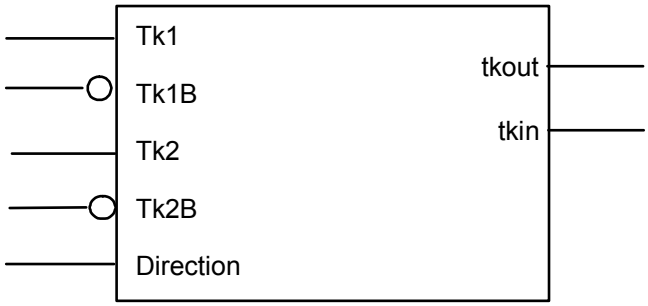

Figure 3-13 Token and Data Inputs circuit

Table 3-38 : Token and Data Input Signal Definitions

Signal Name	Active State/Edge	Function
tk1		1st Token Port (“Bot”)
tk1B		Complement of above
tk2		2nd Token Port (“Top”)
tk2B		Complement of above
Direction		When Low tk1/tk1b are inputs, tk2/tk2B are outputs When High tk1/tk1b are outputs, tk2/tk2B are inputs
tkin		(internal) Token input
tkout		(internal) Token output

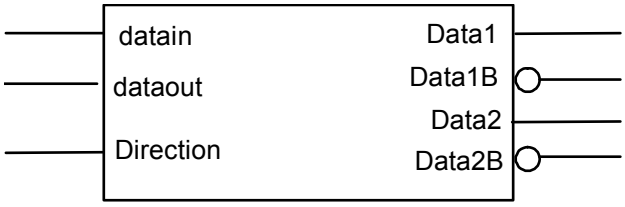

Figure 3-14 Data Ports circuit

Table 3-39 : Token and Data Output Signal Definitions.

Signal Name	Active State/Edge	Function
datain		Data in (internal)
dataout		Data out (internal)
Direction		When Low data1/data1B are ouputs, data2/data2B are inputs When High data1/data1B are inputs, data2/data2B are outputs
data1		1st Data Port (“Bot”)
data1B		Complement of above
data2		2nd Data Port (“Top”)
data2B		Complement of above

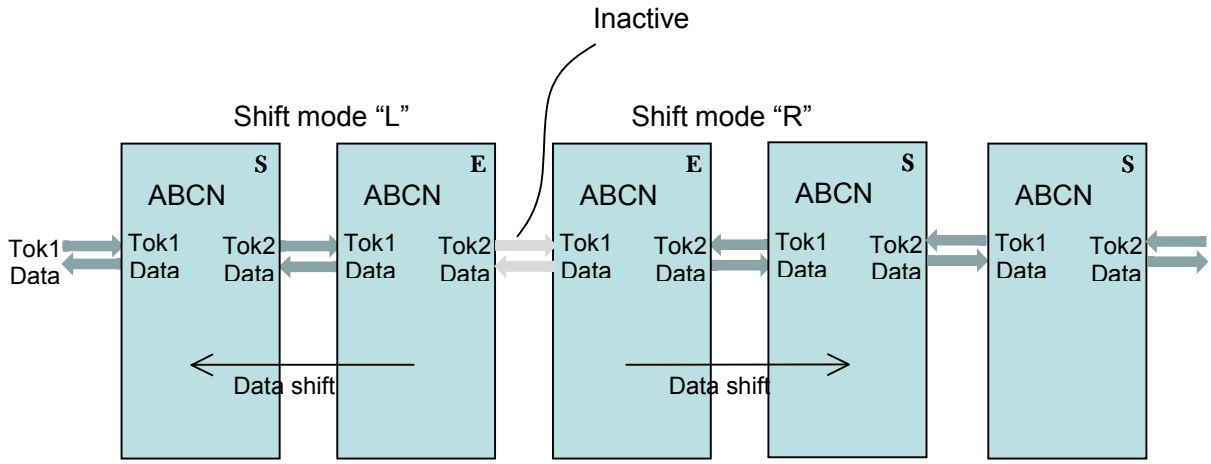

Figure 3-15 Token and Data flows, no chip failure

On Figure 3-15 all ABCN are readable. Three chips are sending data to the left side while two other chips send their data to the right side. In this configuration all chips could be set to send their data to the right or to the left.

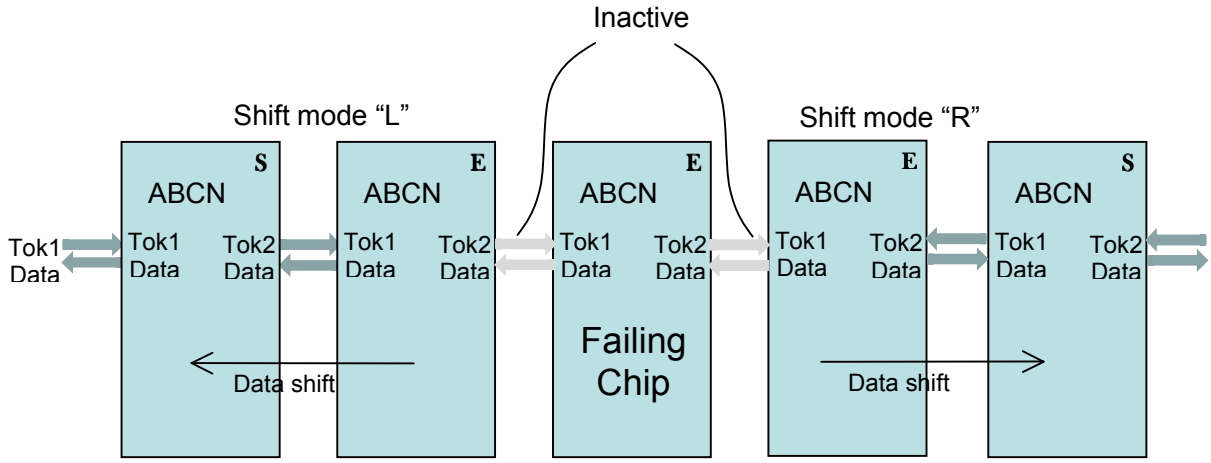

Figure 3-16 Token and Data Flow, one chip failure

On Figure 3-16 one of the ABCN has a failure. It can be excluded from the daisy chain readout by setting the two chips on the left to send their data to the left side while the two chips at right send their data to the right side. In this configuration there is no anymore choice to read any chip from left or right side.

3.2.15 Calibration logic

The calibration logic produces a calibration pulse signal for the front-end calibration circuit. This pulse is produced in response to a control command ”CalPulse”. A two-bit calibration code is also sent to the calibration circuit which selects one of the four possible patterns in the front-end (Bits 2 and 3 of the Configuration 1 register). The calibration pulse signal must be sent to the front-end a fixed number of clock pulses after receipt of the control command. The delay from the rising edge of the clock signal to the rising edge of the calibration pulse signal is determined by the value loaded into the Calibration Delay Register. This delay can be adjusted in 64 equal steps over a range of 50 ns.

Table 3-40 : Calibration Codes

Cal Pulse	Cal Mode Bit 1	Cal Mode Bit 0	Channels of front-end pulsed
0	X	X	Calibration disabled
1	0	0	in3, in7 in11,...in127
1	0	1	in2, in6 in10,...in126
1	1	0	in1, in5 in9,...in125
1	1	1	in0, in4 in8,...in124

3.2.16 Test Circuitry

To simplify the testing of the chip during production and module assembly, it is proposed that a JTAG logic is implemented. Memory blocks used for the pipeline and the derandomizer have Built_in Self-Test features which raise flags in the Status Register 1 if the self-tests show a failure.

3.2.17 Readout Protocols

3.2.17.1 Module Data

This type of data packet is sent by the ABC-N chip set as “Master”. The packet consists of 3 elements, a 13-bit header generated by the Master ABC-N chip, a string of physics data packets, from the all ABC-N chips daisy-chained together including the Master ABC-N chip, and a 17-bits trailer transmitted by the ABC-N chip set in “End” mode.

Preamble	DT	LVL1	BC	Sep	Data	Data	Data	Trailer
11101	0	nnnn	bbbbbbbb	1	<block_1>	.....	<block_n>	1000 0000 0000 0000 0
		MS bit First	MS bit First					

Figure 3-17 Module Data Format.

3.2.17.2 DT(Data Type)

The value of this bit determines the type of data which follows. This can either be L1 Trigger Data (DT=0) or Information Data (DT=1). In the case of the ABC-N chip only L1 trigger Data is Sent and hence this field is always set to '0'.

3.2.17.3 L1

Current count of L1 Trigger modulo 16 since the last system reset. This field can be used for event building by the DAQ and also to monitor for lost data.

3.2.17.4 Beam Crossing Number

Current count of Beam Crossing modulo 256 since the last system reset or BC Reset command. It is intended to monitor for clock pulses lost by the on-detector electronics and can be used to tag one beam crossing out of the complete ring of the LHC.

3.2.17.5 Data Block

This is the data packet set from each chip including the master chip. This data block can be any of the four following types, Physics Data, No-Hit Data, Error Data or Configuration Data.

3.2.17.6 Physics Data

This type of data packet is used to send the compressed hit data from the detector. The format of this data is a series of one or more data packets.

Data Packet	Data Packet	Data Packet	Data Packet
<block_1>	<block_2>	<block_i>	<block_n>

Figure 3-18 Physics Data Format

There are 2 types of data_packet, isolated hit packet and non-isolated hit packet. A physics data packet can consist of any combination of these 2 types of packet.

3.2.17.7 Isolated Hit Data-Packet.

This type of packet is used to send the hit information from a hit channel on a chip when non of it's neighbouring channels have been hit.

Isolated Hit Data Packet				
Header	Chip Address	Channel Address	Sep	Hit Pattern
01	aaaaaaa	ccccccc	1	ddd
	MSB First	MSB First		MSB First

Figure 3-19 Isolated hit data packet

Notice the 7 bits field address (ABCD = 4 bits)

3.2.17.8 Non Isolated Hit Data-Packet

This type of packet is used to send data from a group of 2 or more adjacent channels which have been hit. Only the channel address of the 1st channel in the group is sent. It should be noted that this will also be the lowest numbered channel in the group. The chip address and channel address's of the other channels can be derived from that of the 1st and hence are not sent.

Non Isolated Hit Data Packet								
Header	Chip Address	First Hit Channel Address	Sep	First Hit Pattern	Sep	Next Hit Pattern	Sep	Last Hit Pattern
01	aaaaaaa	ccccccc	1	ddd	1	ddd	1	ddd
	MSB First	MSB First		MSB First		MSB First		MSB First

Figure 3-20 Non isolated hit data packet (readout data format)

aaaaaaa	7 bits of the chips geographical address (ABCD = 4 bits)
ccc,cccc	7-bit address of the channel on which the hit or 1st channel in a groups of hits was found
	(See Figure TBD for the physical location of channel addresses.)
ddd	Is the 3 bit hit pattern read out from the hit channel. (Previous, Current, Next)

Example

The following physics data packet would be send out from a chip with a geographical address of $0D and hits on channels 3, 5 and 6.

Header	Chip Address	Isolated Hit Channel Address	Sep	Channel 3 Hit Pattern	Header	Chip Address	Sep	Channel 5 Hit Pattern	Sep	Channel 6 Hit Pattern
01	0001101	0000011	1	ddd	01	0001101	1	ddd	1	ddd
	MSB First	MSB First		MSB First		MSB First		MSB First		MSB First

Figure 3-21 Non isolated hit data packet (example)

3.2.17.9 No Hit Data

If a chip has received the event currently being read out but has not found any hit channels, it outputs a No Hit Data Packet.

Data Packet
001

Figure 3-22 No Hit Data Packet

3.2.17.10Configuration Data 1 (sendID mode)

Configuration data is sent by the chip in response to a L1 trigger when the chip is in its Send_ID mode and the chip did not receive a specific register read command. A packet of data is sent from the chip which contains the chips address and the contents of the chips configuration register 1.

Configuration Data Packet						
Header	Chip Address	Sep	MSB Byte of Config Pattern	Sep	LSB Byte of Config Pattern	Sep
000	aaaaaaa	111	dddddddd	1	dddddddd	1
	MSB First		MSB First		MSB First	

Figure 3-23 Configuration Data Packet

Notice the 7 bits field address (ABCD = 4 bits)

3.2.17.11Register Readout (Read Register mode)

Registers data is sent by the chip in response to a L1 trigger when the chip receives a read register command. A packet of data is sent from the chip which contains the chip address, the register address and the contents of the register.

Register Data Packet							
Header	Chip Address	Sep	Register Address	MSB Byte of Register Data	Sep	LSB Byte of Register Data	Sep
000	aaaaaaa	010	rrrrr	dddddddd	1	dddddddd	1
	MSB First		MSB First	MSB First		MSB First	

Figure 3-24 Read Register Packet

Notice the 7 bits field address (ABCD = 4 bits)

The following table resumes the read registers address (ccccc as C5..C1 in Field 5 of Table 3-43 and Table 3-44).

Table 3-41 : Read Register Address

rrrrr	
000 00	Configuration Register 1
001 00	Mask Register
010 00	Calibration Delay Register
011 10	Calibration Amplitude Register
011 00	Threshold Registers
111 00	Bias Register 1
111 01	Bias Register 2
111 10	Bias Register 3
000 10	TrimDac
001 10	Configuration Register 2
010 10	Latency Register
101 10	Status Register 1
110 10	Status Register 2

3.2.17.12Error Data

Error data is only sent if the chip detects an error, e.g. Buffer overflow. In this cases a data packet of the following format is sent:

Error Data Packet			
Header	Chip Address	Error Code	Sep
000	aaaaaaa	eee	1
	MSB First		

Figure 3-25 Error Data Format

Notice the 7 bits field address (ABCD = 4 bits)

3.2.17.13Error Codes:

2 codes have been defined :

eee = 001 No Data Available (The chip has not received an L1 command)

eee = 100 Buffer Overflow (Soft Reset needed)

N.B. Error messages are only sent if the chip is in Data_Taking mode

3.2.18 Control Protocol

There are two main classes of commands, L1 Trigger Commands and Control Commands, and there are two types of Control Commands, Fast Control Commands and Slow Control Commands. It is not expected that the Slow Control Commands will be issued during data taking operation.

Table 3-42 : Commands

Type	Field 1	Field 2	Field 3	Description
Level 1	110	---	---	L1 Trigger
Fast	101	0100 or 0010		Soft Reset BC Reset
Slow	101	0111	Command	Slow Control Command, see Table 3-43 and Table 3-44

3.2.18.1 L1 trigger Command:

This is the most frequently issued packet and hence the smallest. All ABC-N chips that receive this packet act on it. There is no addressing. If this command is received 3 samples are readout out of the pipeline and written into the readout buffer.

3.2.18.2 Fast Control Command:

This type of command is sent when a command has to be issued to the chip more quickly than can be achieved by sending a slow command to the chip. In the case of the ABC-N chip, only two commands of this type have been defined, i.e. the Soft Reset and BC Reset commands. It is expected that these commands will be sent to the chip at regular intervals during periods of time when no L1 Triggers will be sent to the chip. The purpose of these commands is to perform a limited reset of the chip. (see section 3.2.19 for details)

3.2.18.3 Control commands

These are long packets that enable the operation of the chip to be controlled. While they are being sent, it is not possible to send a L1 trigger. Only the addressed ABC-Ns will act on the packet, unless the address sent equals '111111', in which case all chips will act on the packet. All chips that receive the packet must decode it, even if they do not act on it. This is to avoid un-addressed ABC-Ns erroneously decoding parts of the data field as the start of packets. To ensure that the chip does not respond to

erroneous commands the chip will be placed out of taking mode for any command it receives which effects the configuration of the chip, i.e. all commands in which the 1st bit of field 5 is '0'. Hence it will be necessary to issue a command to the chip to enable data taking after issuing a command to change its configuration. When the chip is not in data taking mode or in read register mode, it will send its ID instead of real data in response to a L1 Trigger. This is the power-on default state.

Table 3-43 : Control Commands (as for ABCD)

Field 3	Field 4	Field 5	Field 6	Description
0001,1100	aaaaaaa	000 000	dddd,dddd,dddd,dddd	Write Configuration Register 1
1000,1100	aaaaaaa	001 000	d---,----,----,---d	Write Mask Register
0001,1100	aaaaaaa	010 000	dddd,dddd,dddd,dddd	Write Calibration Delay Register
0001,1100	aaaaaaa	011 000	dddd,dddd,dddd,dddd	Write Threshold Registers
0000,1100	aaaaaaa	100 000	----------	Instr. Test Pulse to Input_Reg
0000,1100	aaaaaaa	101 000	----------	Instr. Enable Data taking Mode
0000,1100	aaaaaaa	110 000	----------	Instr. Issue Calibration Pulse
0001,1100	aaaaaaa	111 000	dddd,dddd,dddd,dddd	Write Bias DAC
0001,1100	aaaaaaa	000 100	dddd,dddd,dddd,dddd	Write TrimDac

Table 3-44 : Additional Control Commands for ABC-N

Field 3	Field 4	Field 5 C5…C0	Field 6	Description
0001,1100	aaaaaaa	000 001	----------	Read Configuration Register 1
1000,1100	aaaaaaa	001 001	----------	Read Mask Register
0001,1100	aaaaaaa	010 001	----------	Read Calibration Delay Register
0001,1100	aaaaaaa	011 001	----------	Read Threshold Registers
0001,1100	aaaaaaa	111 001	----------	Read Bias Register 1
0001,1100	aaaaaaa	000 101	----------	Read TrimDac
0001,1100	aaaaaaa	111 010	dddd,dddd,dddd,dddd	Write Bias Register 2
0001,1100	aaaaaaa	111 011	----------	Read Bias Register 2
0001,1100	aaaaaaa	111 100	dddd,dddd,dddd,dddd	Write Bias Register 3
0001,1100	aaaaaaa	111 101	----------	Read Bias Register 3
0001,1100	aaaaaaa	001 100	dddd,dddd,dddd,dddd	Write Configuration Register 2
0001,1100	aaaaaaa	001 101	----------	Read Configuration Register 2
0001,1100	aaaaaaa	010 100	dddd,dddd,dddd,dddd	Write Latency Register
0001,1100	aaaaaaa	010 101	----------	Read Latency Register
0001,1100	aaaaaaa	011 100	dddd,dddd,dddd,dddd	Write Calibration A. Register
0001,1100	aaaaaaa	011 101	----------	Read Calibration A. Register
0001,1100	aaaaaaa	101 101	----------	Read Status Register 1
0001,1100	aaaaaaa	110 101	----------	Read Status Register 2

N.B.

xxx = don't care state**.**

aaaaaaa = 7 bits chip address(MS bit first)

dddd = data value for register (MS bit first)

Field 3

This is an 8 bit count of the number of bits in the following instruction.

Field 4

This is the 7-bit address of the chip for which the command is intended. (See Section on Geographical Address). The field size was 4 bits in case of the ABCD chip. The compatibility with the DAQ system should be checked.

Field 5

This 6 bit field is used to determine into which register on the chip the data contained in the following field will be written or which command sequence is to be executed.

Field 6

This field holds the data that is to be written into the selected register. With the exception of instructions which load the mask register, this field will be 16-bits long.

3.2.19 Chip Initialisation and Configuration

The chip has 3 modes of operation, "Send_ID Mode", “Read Register Mode” and "Data_Taking Mode". After a Power-up reset the chip is placed into Send_ID mode.

3.2.19.1 Send_ID Mode

In this mode of operation the chip sends its ID and Configuration data in response to a L1 trigger. There is no command which explicitly places the chip into this mode of operation, however, any attempt to alter the contents of the chip's various registers (write operation) automatically results in the chip being placed into Send_ID mode.

3.2.19.2 Data_Taking Mode.

The chip is placed in this mode of operation by sending a command to the chip to enable data taking. In this mode of operation the chip sends out any physics data that it has. The chip is taken out of this mode of operation and placed into Send_ID mode by either a Power_up reset or any attempt to change the contents of the chip's registers. The chip is taken out of this mode of operation and placed into the Read Register mode by any read register command.

3.2.19.3 Clock Feed Through

If the clock feed through bit in the configuration register has been cleared and the chip has been configured as a Master, the chip outputs the chip system clock divided down by 2 from it’s data output pins. This feature has been included to simplify system testing.

3.2.20 Resets

There are three kinds of reset in the system.

3.2.20.1 Power up reset

The power-up reset is an asynchronous (i.e. clock independent) reset that sets the value of the chips registers to their default value, and clears all the buffers in the chip, thus placing the chip into a well defined state. This type of reset is issued automatically when power is first applied to the chip. Provision will be made to enable this signal to be supplied externally to the chip.

3.2.20.2 Soft Reset

This type of reset is sent to the chip via a command instruction. Its purpose is to clear all the buffers in the chip, while leaving the configuration of the chip unaffected. This type of reset will be issued to the chip periodically during data taking to eliminate synchronisation errors.

1) Upon receipt of the Soft Reset command, the ABC-N chip resets all internal counters, clears tokens and sets itself to the no-data state. If it was transmitting data, it terminates this immediately.

2) The external system must wait a time consistent with any data in the serial chain at the reset clock cycle to flush through the chain. This is one clock cycle per chip in the read-out chain, or 0.3µs for a 12 chip ring.

N.B. It should be noted that the off-detector system must then be able to determine the last complete event transmitted before the reset and discard it (Complete in the sense that all read-out chains supply a header and trailer). With either reset it must also be able to recognise and discard partial events since there is no guarantee that different read-out chains will be reading the same event when the periodic reset arrives. This section will define how the chip behaves on power up, i.e. default state of registers etc. latch-up prevention measures needed , and any special power cycling or power ramping required.

3.2.20.3 BC Reset

This type of reset is sent to the chip via a command instruction. Its purpose is to zero the Beam Crossing counter. It has no effect on the operation of any other part of the chip.

The following sequence of instructions should normally be sent to the chip after power-up

1) Send command to load the configuration register with the appropriate settings.

2) Send a command to load the mask register

3) Send a series of commands to load the DAC register/s and Delay registers

4) Send a command to place the chip into data taking mode.

The chip will now be in a state to receive L1 trigger command and send data.

3.2.21 Default Register Values

On power up, the contents of the configuration register will be set to zero. This results in the following configuration.

Data compression is set to Detector alignment mode (see Table 3-7 : Data Compression Criteria)

Calibration Mode is disabled

Send_ID mode is enabled.

tokin0 and din0 inputs are enabled

tokout0 and dout0 outputs are enabled.

Input test mode is disabled.

Edge Detection Mode disabled

Clock Feed Through Mode is Enabled if the chip is acting as a Master.

Chip will not be configured as the end of a readout chain.

The chip will be configured as a Master if masterB is asserted, else it will be configured as a slave.

3.2.22 Master/Slave Selection

The default state of the chip on power up is determined by the state on the masterB input pin. If this pin has been left unconnected or tied high, the chip will powered up as a Slave. If this pin has been tied to ground, the chip will powered up as a Master. If the chip is configured as a Master on power up it may be re-configured as a slave.

3.2.23 Input/Output Connections

The following tables describe the names and function of the various Input/Output connections to the chip.

Table 3-45 : Digital Input Signals

Name	Function	Type
clk0 & clk1	Readout Clock	LVDS
clk0B & clk1B	Complement of above signal	LVDS
BC0 & BC1	Main clock input	LVDS
BC0B & BC1B	Complement of above signal	LVDS
com0 & com1	Command Input	LVDS
com0B & com1B	Complement of above signal	LVDS
Lone0 & Lone 1	Command Input	LVDS
Lone 0B & Lone 1B	Complement of above signal	LVDS
Tk1 & Tk2	Token Input/Ouput	LVDS, Bidirectional
Tk1B & Tk2B	Complement of above signal	LVDS, Bidirectional
Data1 & Data2	Data Input/Output	LVDS, Bidirectional
Data1B & Data2B	Complement of above signal	LVDS, Bidirectional
id<6:0>	Geographical address of chip	CMOS
masterB	Sets chip default to master	CMOS
select	Selects clock/command inputs	CMOS
ClkMode80	Sets chip for 80MHz readout	CMOS
ClkMode160	Sets chip for 160MHz readout	CMOS
ShuntE	Enable of internal Shunt Reg.	CMOS
REGenable	Enable of serial Regulator	CMOS
HardresetB	Resets Chip	CMOS

Table 3-46 : Default settings of CMOS input signals

Name	Function	Default setting
id<6:0>	Geographical address of chip	High, pull-up with 100 kOhm
masterB	Sets chip default to master	High, pull-up with 100 kOhm
select	Selects clock/command inputs	Low, pull-down with 100 kOhm
ClkMode80	Sets chip for 80MHz readout	High, pull-up with 100 kOhm
ClkMode160	Sets chip for 160MHz readout	High, pull-up with 100 kOhm
ShuntE	Enable of internal Shunt Reg.	High, pull-up with 100 kOhm
REGenable	Enable of serial Regulator	High, pull-up with 100 kOhm
resetB	Resets Chip	High, pull-up with 100 kOhm

Table 3-47 : Digital Output Signals

Name	Function	Type
Tk1 & Tk2	Token Input/Ouput	LVDS, Bidirectional
Tk1B & Tk2B	Complement of above signal	LVDS, Bidirectional
Data1 & Data2	Data Input/Output	LVDS, Bidirectional
Data1B & Data2B	Complement of above signal	LVDS, Bidirectional
Ldo	Data Output of "Master" chip	LVDS
LdoB	Complement of above	LVDS

3.2.24 DC Supply and Control Characteristics:

The DC supply voltages requirements as defined below apply to the core of the ABC-N chip and will be delivered either from the internal on chip power management circuitry or from the external power sources via bond pads.

Table 3-48 : DC supply voltages

	Pad Name	Min	Nominal	Max	Absolute Max
Analogue Supply*	VDDA	2.1 V	2.2 V	2.3 V	2.7 V
Analogue Ground	VSSA		0 V		
Input transistor bias current**	set from internal DAC	27 µA	40 µA	66 µA	
Preamplifier feedback bias current***	set from internal DAC	1.8 µA	3 µA	11 µA	
Preamplifier buffer bias current	set from internal DA	5.4 µA	8 µA	13.2 µA	
Shaper bias current	set from internal DAC	5.4 µA	8 µA	13.2 µA	
Shaper feedback bias current	set from internal DAC	5.4 µA	8 µA	13.2 µA	
Differential stage bias current	set from internal DAC	18 µA	30 µA	44 µA	
Comparator bias	set from internal DAC	18 µA	30 µA	44 µA	
Discriminator threshold	VTHP	0 µA	0 µA	0 µA	VDDA
Discriminator threshold	VTHN	0 µA	0 µA	0 µA	VDDA
(Vthp - Vthn)		0	90 mV	816 mA	0 to 1 V
Digital Supply#	VDDD	2.4 V	2.5 V	2.6 V	2.7 V
Digital Ground	VSSD		0 V		

* DC supplies are the one applied to the analogue circuits, from either an output source or from the internal analogue voltage regulator.

** Multiplied by 3 in every channel

*** Divided by 10 in every channel

DC supplies are the one applied to the digital circuits, from either an output source or from the internal digital voltage regulator. For the on chip power-up reset to operate correctly the VDD power supply must be ramped up to 90% of its final value in less than 10 ms.

The current draw at each DC input is as follows (values excluding the regulators current).

Table 3-49 : DC supply currents for the nominal voltage supplies (VDDA=2.2V, VDDD=2.5V) and nominal operating conditions

		Min	Nominal	Max
Analogue Supply	VDDA	21 mA	27 mA	43 mA
Analogue Ground	VSSA	-21 mA	-27 mA	-46 mA
Digital Supply*	VDDD	46 mA	92 mA	138 mA
Digital Ground	VSSD	-46 mA	-92 mA	-138 mA

*In the Master chip the current draw at VDDD power supply will be approximately 4 mA higher compared to the values shown in the table.

Table 3-50 : Absolute Min/Max current draws at power supply inputs which may occur in non-standard operating conditions, e.g. all bias DACs set at zero or to full range, clock not supplied to the chips

		Min	Nominal	Max
Analogue Supply	VDDA	21 mA	27 mA	43 mA
Digital Supply	VDDD	10 mA (14 mA)*	92 mA (96 mA)*	138 mA (142 mA)*

*Current draws by the Master chip

3.2.25 Power Consumption

Expected typical power consumption for nominal bias power supply voltages and bias currents: 2.3 mW/channel.

3.2.26 Input/Output Levels

Table 3-51 : Input Levels for LVDS Inputs (Clock, BC, Command, Lone)

Parameter	**Conditions**	**Minimum**	**Maximum**
Input Voltage Range V_i	VDDD=2.5V	0 mV	2400 mV
InputVoltage Common mode V_{icm}	VDDD=2.5V	50 mV	2350 mV
Differential high input threshold $+V_{idth}$	VDDD=2.5V		100 mV
Differential high input threshold $-V_{idth}$	R_{load} =100Ω ±1%	-100 mV	
Threshold hysteresis			
Receiver input impedance		100 kΩ	

N.B. No internal terminating resistor is built into these inputs and consequently an external resistor terminated resistor is required.

Table 3-52 : Input Levels for special Inputs (Bidirectional token, data)

Parameter	Conditions	Minimum	Maximum
Input Voltage Range V_i	VDDD=2.5V	0 mV	2400 mV
InputVoltage Common mode V_{icm}	VDDD=2.5V	50 mV	2350 mV
Differential high input threshold $+V_{idth}$	VDDD=2.5V		100 mV
Differential high input threshold $-V_{idth}$	R_{load} =100Ω ±1%	-100 mV	
Threshold hysteresis			
Receiver input impedance		100 Ω	

The parameters for the token/data I/O are not fully defined in the present document. When the token or data are used as inputs, the input impedance of the receiver part is set low, The drive capability of the driver part is disabled (high impedance state) The power consumption of the driver part is reduced.

Table 3-53 : Output Levels for LVDS Outputs (Ldo)

Parameter		Minimum	Maximum
Output Voltage low V_{OL}	R_{load} =100Ω ±1%	1000 mV	
Output Voltage High V_{OH}	R_{load} =100Ω ±1%		1400 mV
Output offset Voltage	R_{load} =100Ω ±1%	1125 mV	1275 mV
Output Differential Voltage	R_{load} =100Ω ±1%	250 mV	400 mV
Output impedance	I_{load} =2mA to 3mA	40 Ω	280 Ω

Table 3-54 : Output Levels for special Outputs (Bidirectional token, data)

Parameter		Minimum	Maximum
Output Voltage low V_{OL}	R_{load} =100Ω ±1%	1000 mV	
Output Voltage High V_{OH}	R_{load} =100Ω ±1%		1400 mV
Output offset Voltage	R_{load} =100Ω ±1%	1125 mV	1275 mV
Output Differential Voltage	R_{load} =100Ω ±1%	250 mV	400 mV
Output impedance	I_{load} =2mA to 3mA	40 Ω	280 Ω

The parameters for the token/data I/O are not fully defined in the present document. When the token or data are used as outputs, the input impedance of the receiver is set high and its power consumption is reduced. The output of the receiver is set to the logical state zero. The output drive capability is controlled through 5 bits set on the Configuration 2 Register. The current ranges from 0 to 6.4mA by steps of 200uA

3.2.27 Shunt and Voltage Regulators

The ABC-N chips will be supplied by a constant current source. The supply voltage for the digital circuits is regulated by the shunt regulator. The supply voltage for the analogue circuit is derived from the output voltage of the shunt regulator and is regulated by the linear regulator. The use of the internal regulators is optional and can be disabled by wire bonding to the pads ShuntE .

The shunt regulators must allow connecting their outputs in parallel on the hybrid even if the output voltages of the individual devices are not perfectly matched. It is required that devices with mismatch of output voltages within a range ±100 mV can be connected in parallel.

3.2.27.1 Shunt regulator

Table 3-55 : Shunt regulator specifications

		Min	Nominal	Max
Reference input voltage	Vbg		1.165 V	
Shunt output voltage for Ishunt = 10 mA	Vout	2.48	2.50 V	2.52
Minimum shunt current	Ishuntmin		2 mA	
Internal shunt current limit Shunt1 and Shunt2 inputs open (default configuration)	Ishuntlimit0	80 mA	100 mA	120 mA
Elevated current limits selectable by bonding Shunt1 nad Shunt2 inputs				
Shunt1=open , Shunt2=VDDD	Ishuntlimit1	120 mA	150 mA	180 mA
Shunt1=VDDD, Shunt2=open	Ishuntlimit2	150 mA	200 mA	240 mA
Shunt1=VDDD, Shunt2=VDDD	Ishuntlimit3	200 mA	250 mA	300 mA
Absolute maximum shunt current (limit set by the current limits of the bond wires and of the power busses)			300 mA	
Disable input	ShuntE		VDDD	
Output impedance Ishunt = 2 mA f < 100 Hz 100 Hz < f < 1 kHz 1 kHz < f < 10 kHz f > 10 kHz Ishunt = 10 mA f < 100 Hz 100 Hz < f < 1 kHz 1 kHz < f < 10 kHz f > 10 kHz Ishunt = 20 mA f < 100 Hz 100 Hz < f < 1 kHz 1 kHz < f < 10 kHz f > 10 kHz				 0.5 Ω 2.5 Ω 40 Ω 65 Ω 0.05 Ω 0.3 Ω 3.0 Ω 8.0 Ω 0.02 Ω 0.15 Ω 1.5 Ω 4.0 Ω
Ramp-up time of the supply current	tramp	0.1 ms		

3.2.27.2 Voltage Regulator for the analogue front-end circuits

Table 3-56 : Analogue voltage regulator specifications

		Min	Nominal	Max
Input Voltage	VDDD	2.48 V	2.5 V	2.52 V
Output voltage	VDDA		2.2 V	
Output current			40mA	50mA
Output Impedance			1.5 Ω @ 10MHz	6.5 Ω
Rejection Ratio			7dB @ 30MHz	
Rejection Ratio with 100nF external capacitor			30dB @ 30MHz	

3.2.28 Physical Requirements

3.2.28.1 Floor plan

The ABC-N chip will be 7.5 mm wide and to fit at best the input pads to the sensor strip pitch, while keeping a reasonable gap between adjacent chips to allow the placement of decoupling capacitors..

A preliminary figure of the pads implementation is shown on Figure 3-26. It does not includes the FE input pads distribution and the pads used only for test/debugging purpose.

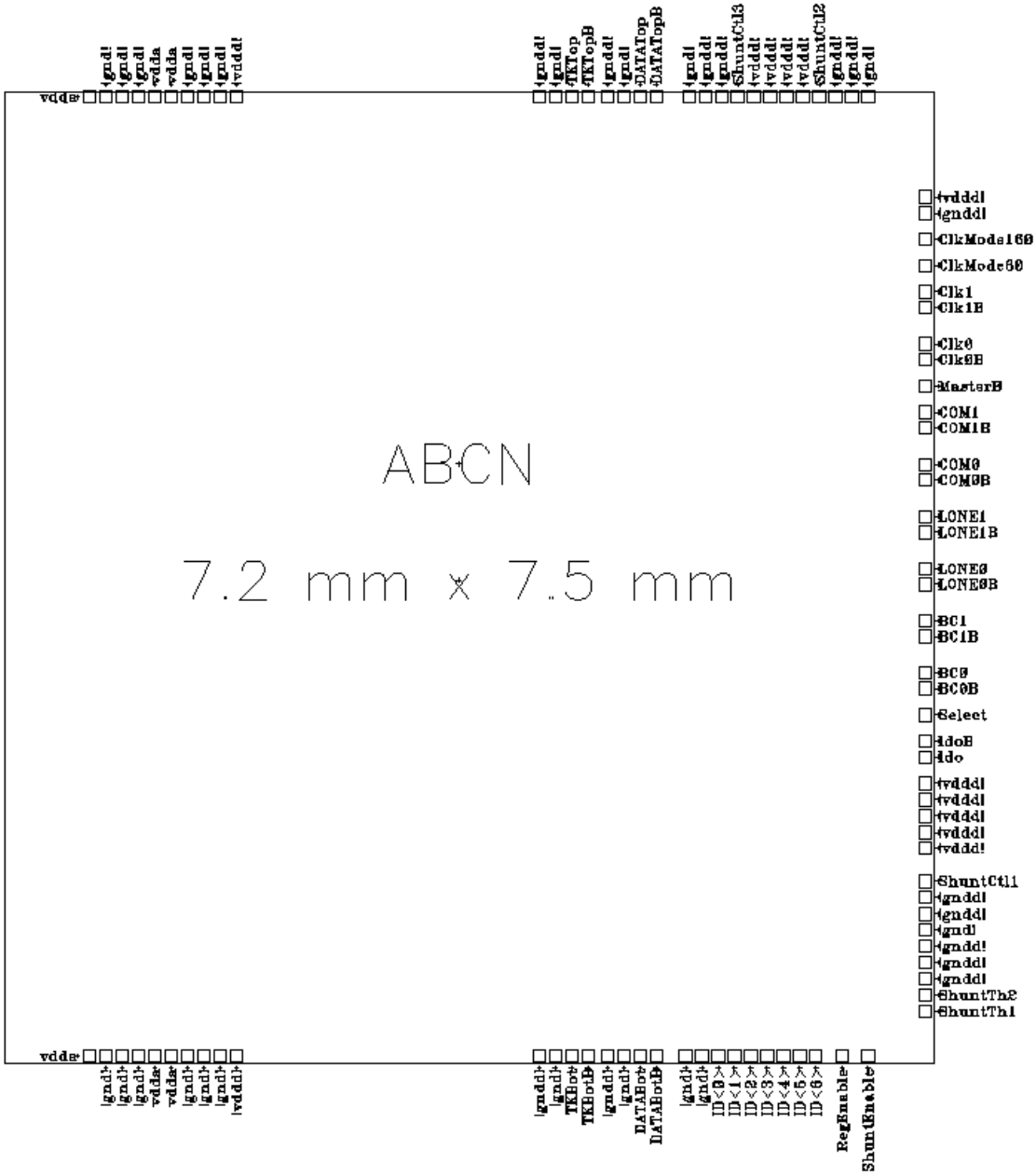

Figure 3-26 Preliminary Pads distribution