BCM FPGA Firmware v4

Code/Design Review

Aleš Svetek
J. Stefan Institute, Ljubljana

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Agenda

- BCM FPGA Main Tasks
- Upgrade v3 ➔ v4
- BCM FPGA Data Flow
- BCM FPGA Firmware v4 Design
- FPGA Resource Utilization
- Design Status

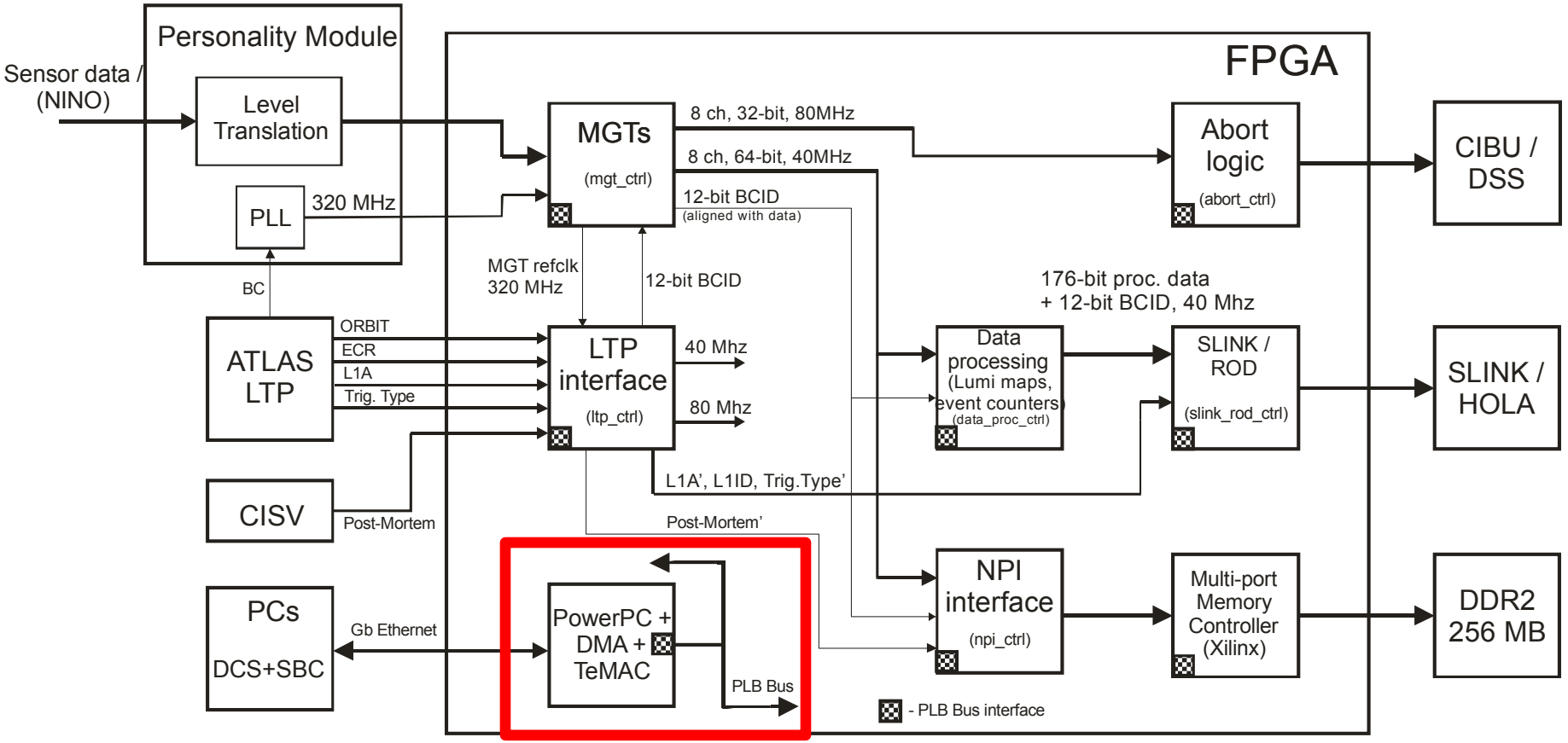
BCM FPGA main tasks

- DAQ of sensor data at 2.56 GHz (64 samples at 390 ps for each BC)
- Beam Monitor ➔ Controls Interlocks Beam User (CIBU) , Detector Safety System (DSS) and Post-Mortem Buffer
- Luminosity Monitor
- TDAQ ROD functionality
- CTP triggers
- Detector Control System (DCS)

BCM FPGA Firmware Upgrade

- On-board (system) MGT synchronization support
- Adapt to channel remapping
  (8 LG channels ➔ Beam_Abort_ROD)
  (8 HG channels ➔ Lumi_ROD)
- Redesign Basic Beam Abort Algorithm
- Redesign CTP trigger outputs
- Integrate Test Vector “play back”
- Gb Ethernet (TCP, UDP) – faster Post-Mortem buffer download
- Prepare only 1 FPGA firmware, final operation defined by SW

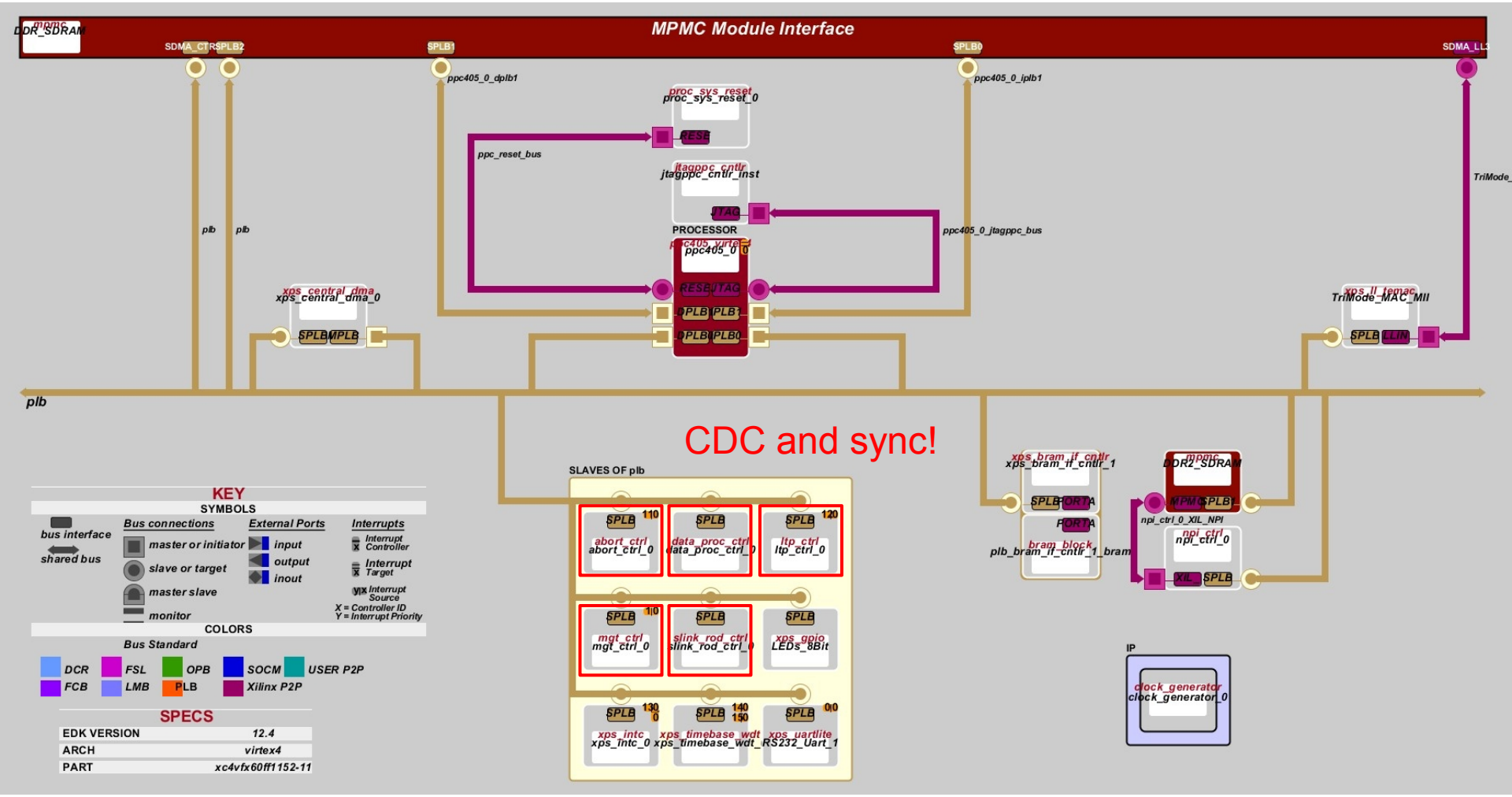
BCM FPGA Data Flow



Why utilize PowerPC 405?

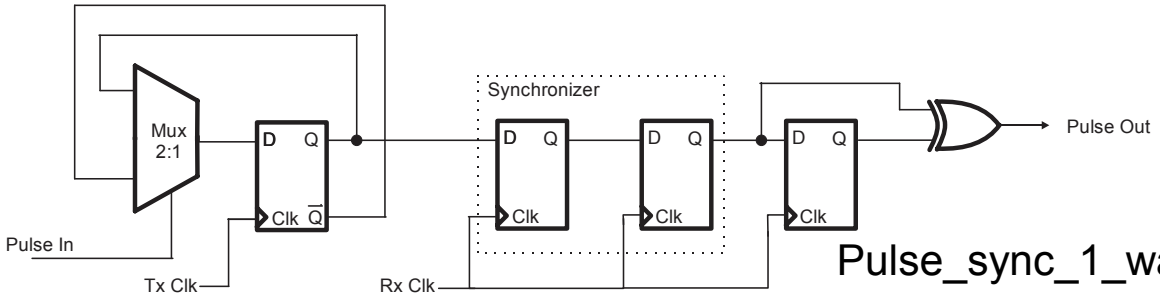
- Support GbE UDP and TCP/IP communication
- Execute the MGT calibration algorithms
- Generate and load MGT test vectors
- Startup Built-in Self Test(BIST), DDR and DDR2 RAM
- Provide additional debug information

Processor System Architecture

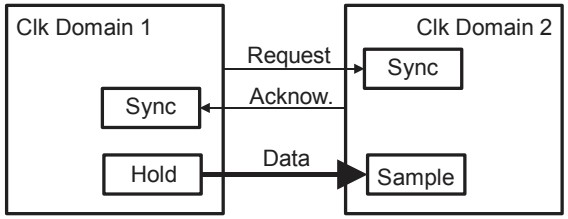


Clock Domain Crossing and Sync.

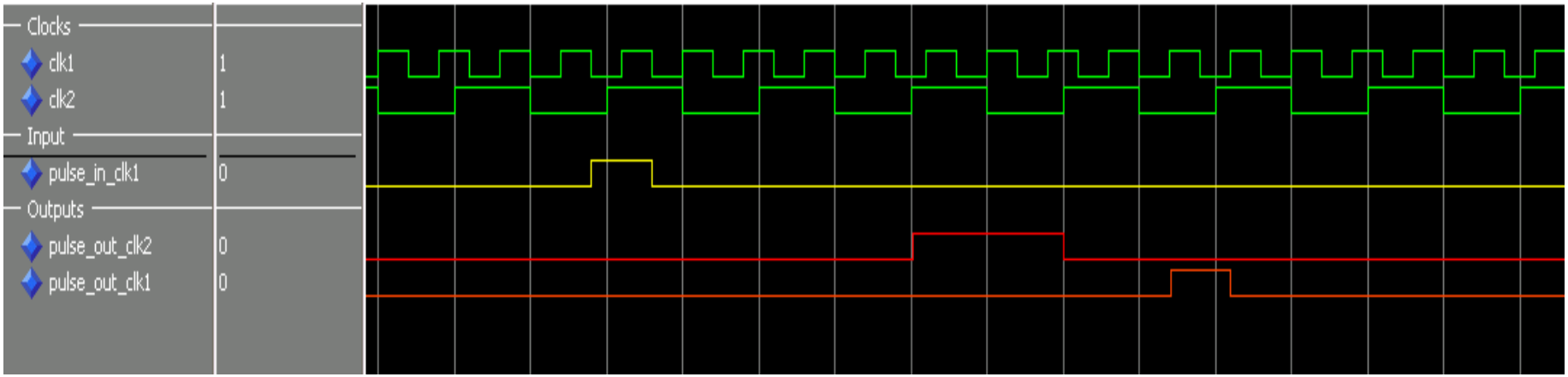
- Edge detector
- 2-stage synchronizer
- Pulse_sync_1_way
- Pulse_sync_2_way
- (FIFOs)



Pulse_sync_1_way



Datapath sync.



Processor Support Modules

- Reset generator (reset sequencing of PPC405, PLB Bus, Peripherals)
- Clock generator (1x 300 MHz, 2x 100 MHz, 2x 200 MHz, 1x 50 MHz)
- JTAG controller
- Interrupt controller (intc)
- UART/RS-232
- Watchdog timer

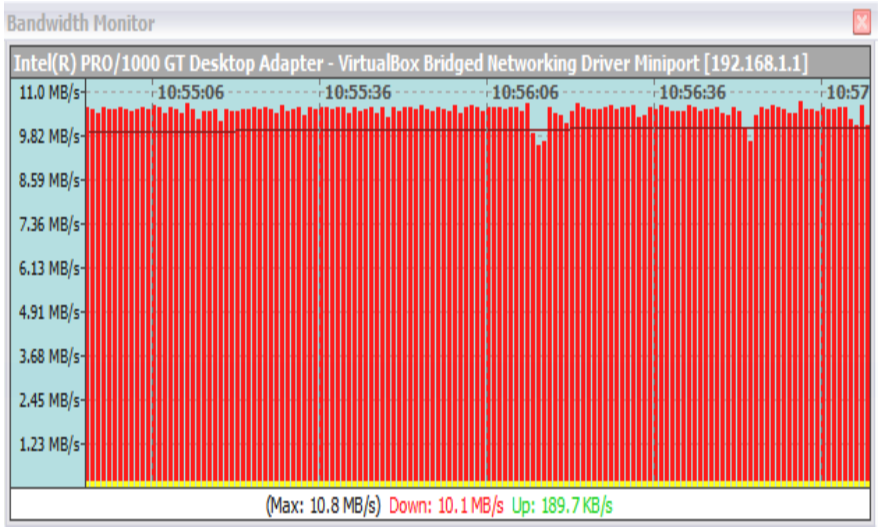
Gb Ethernet Communication

- Available well-known socket communication APIs
- Post-Mortem buffer dump
- Startup parameter configuration from OKS
- DCS slow control
- Syslog daemon channel
- Command-line/Telnet interface to PPC (used to read/write to any register, parameter reconfiguration, diagnostics)

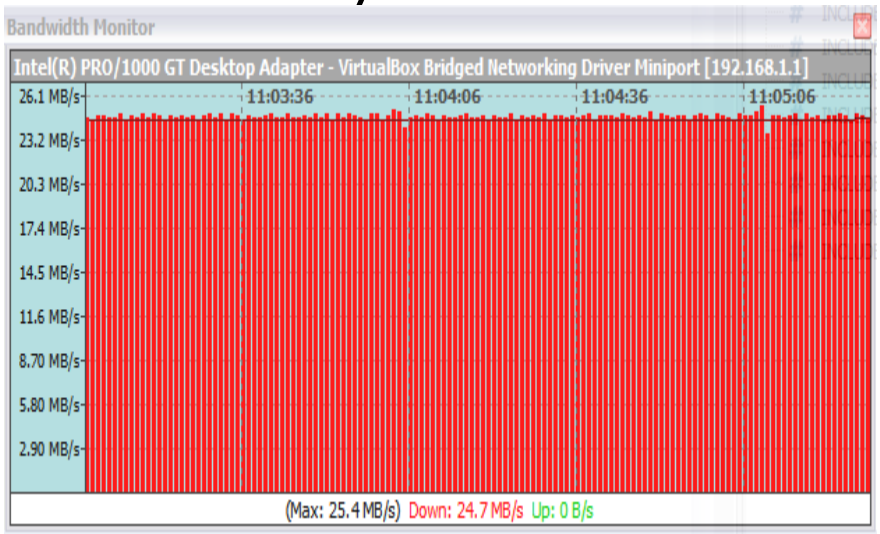
Gb Ethernet throughput (LWIP)

- Benchmark: **iperf** application for measuring maximum TCP and UDP bandwidth performance
- Using MTU **1500** (Maximum Transmission Unit)
- Using open-source **LWIP** (Lightweight IP) stack: sustained throughput (BCM FPGA ➔ PC)

11 MB/s via TCP



25 MB/s via UDP

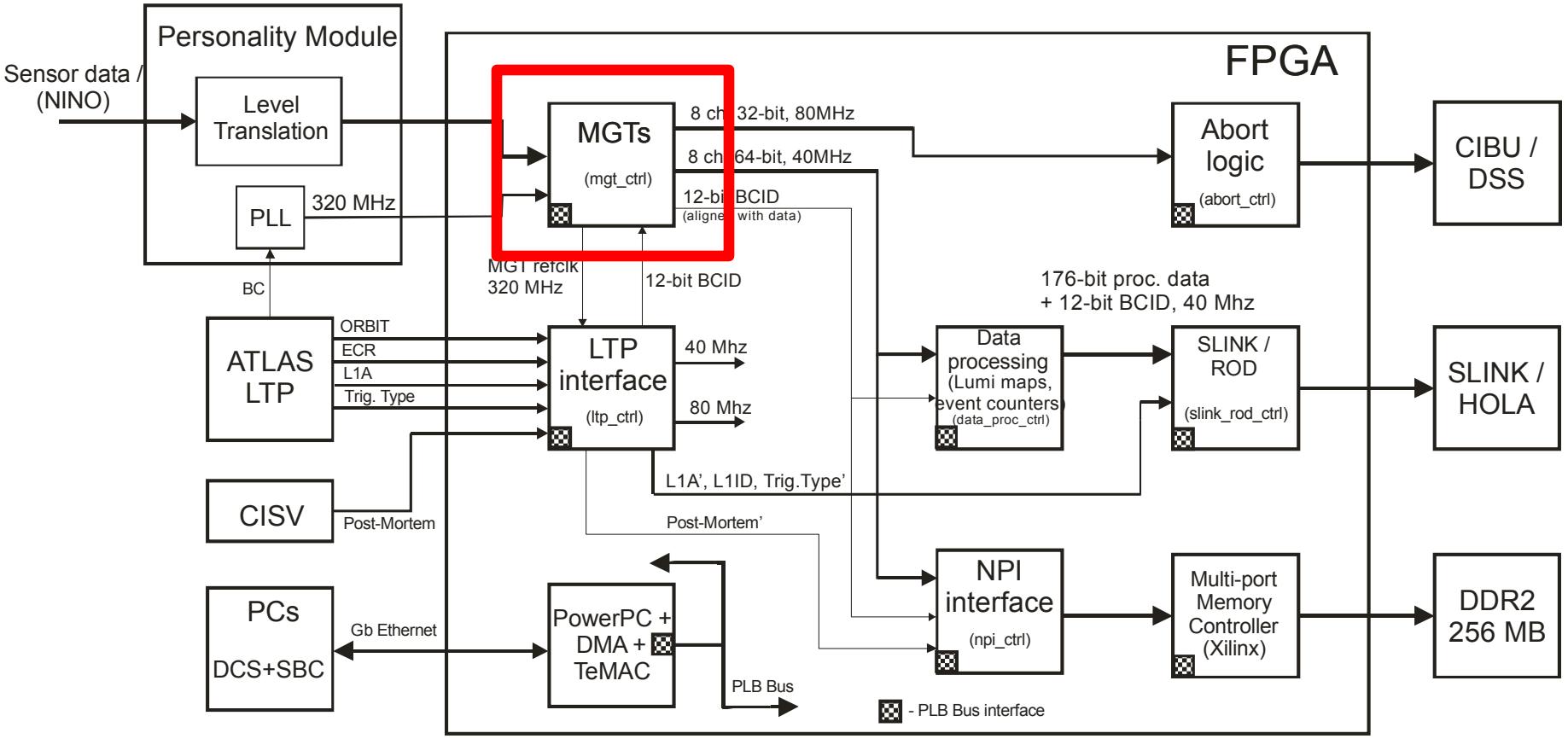


Gb Ethernet throughput (Treck Inc.)

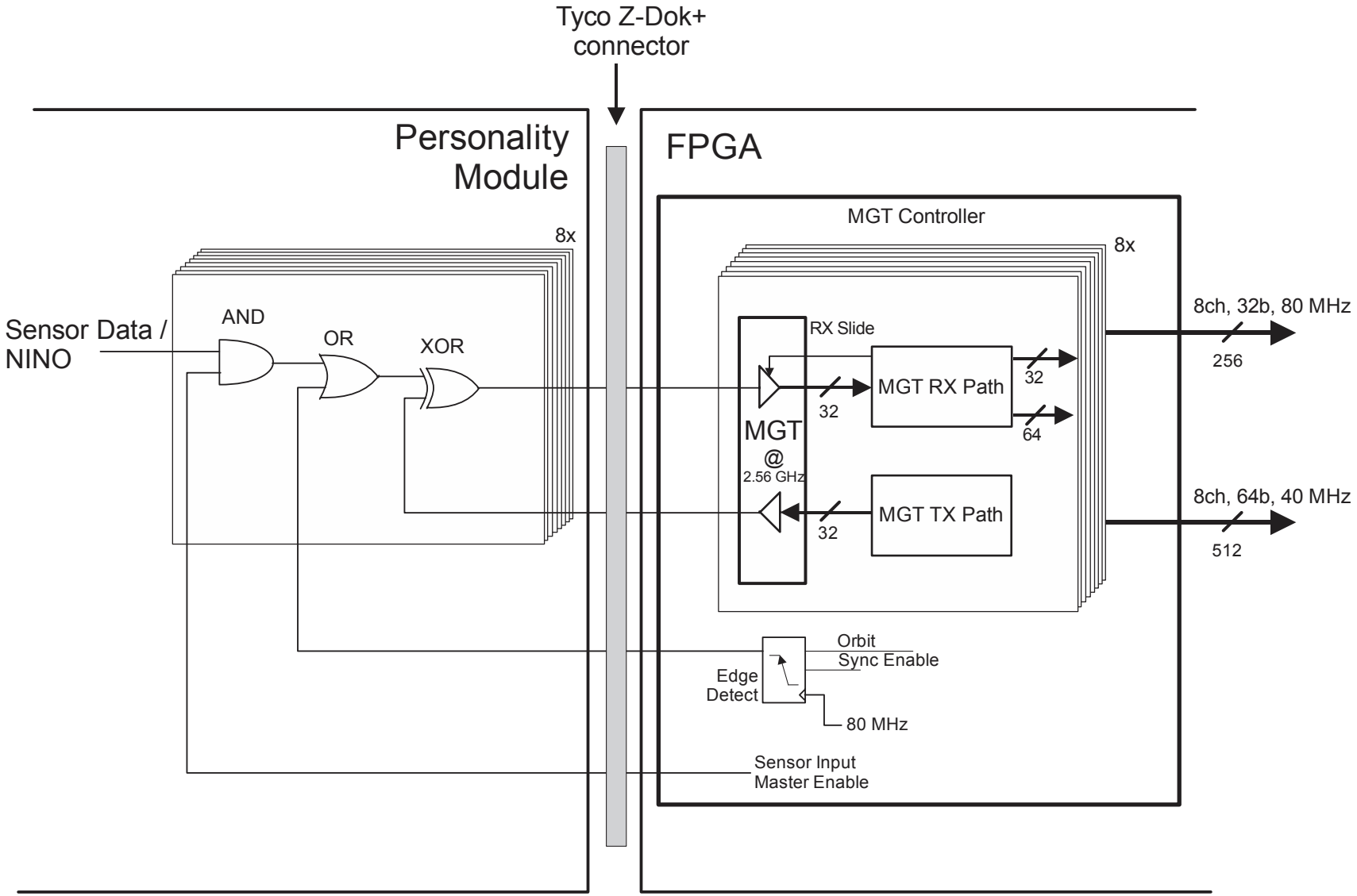
- Commercial TCP/IP stack solution
- **Using the same FPGA hardware:**
  - MTU 1500 ➔ 27 MB/s (213 Mbps) via TCP
  - MTU 9000 ➔ 115 MB/s (922 Mbps) via TCP
- Price: 20.000 €

Source: Xilinx Application Note XAPP1043: Measuring Treck TCP/IP Performance Using the XPS LocalLink TEMAC in an Embedded Processor System

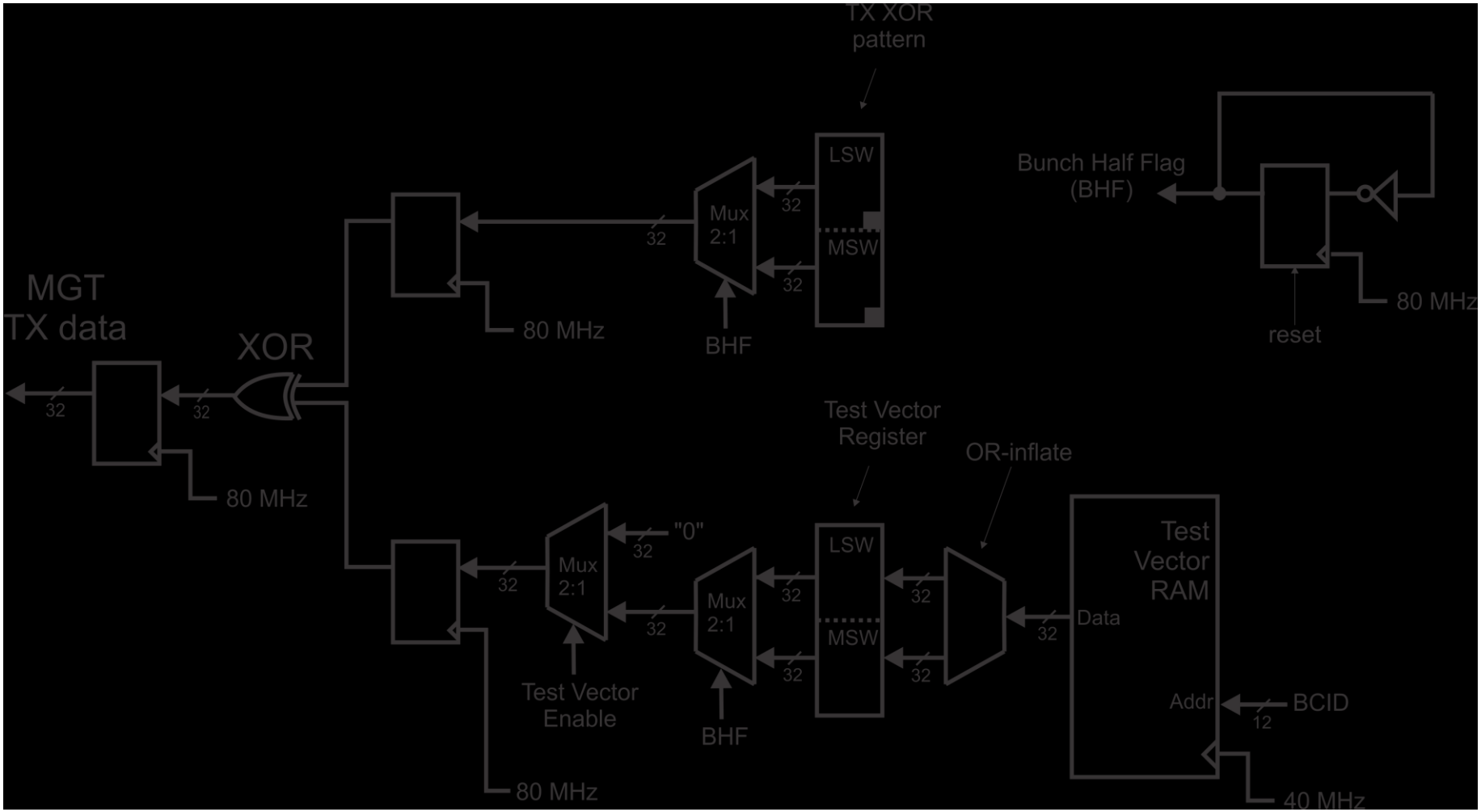
BCM FPGA Data Flow



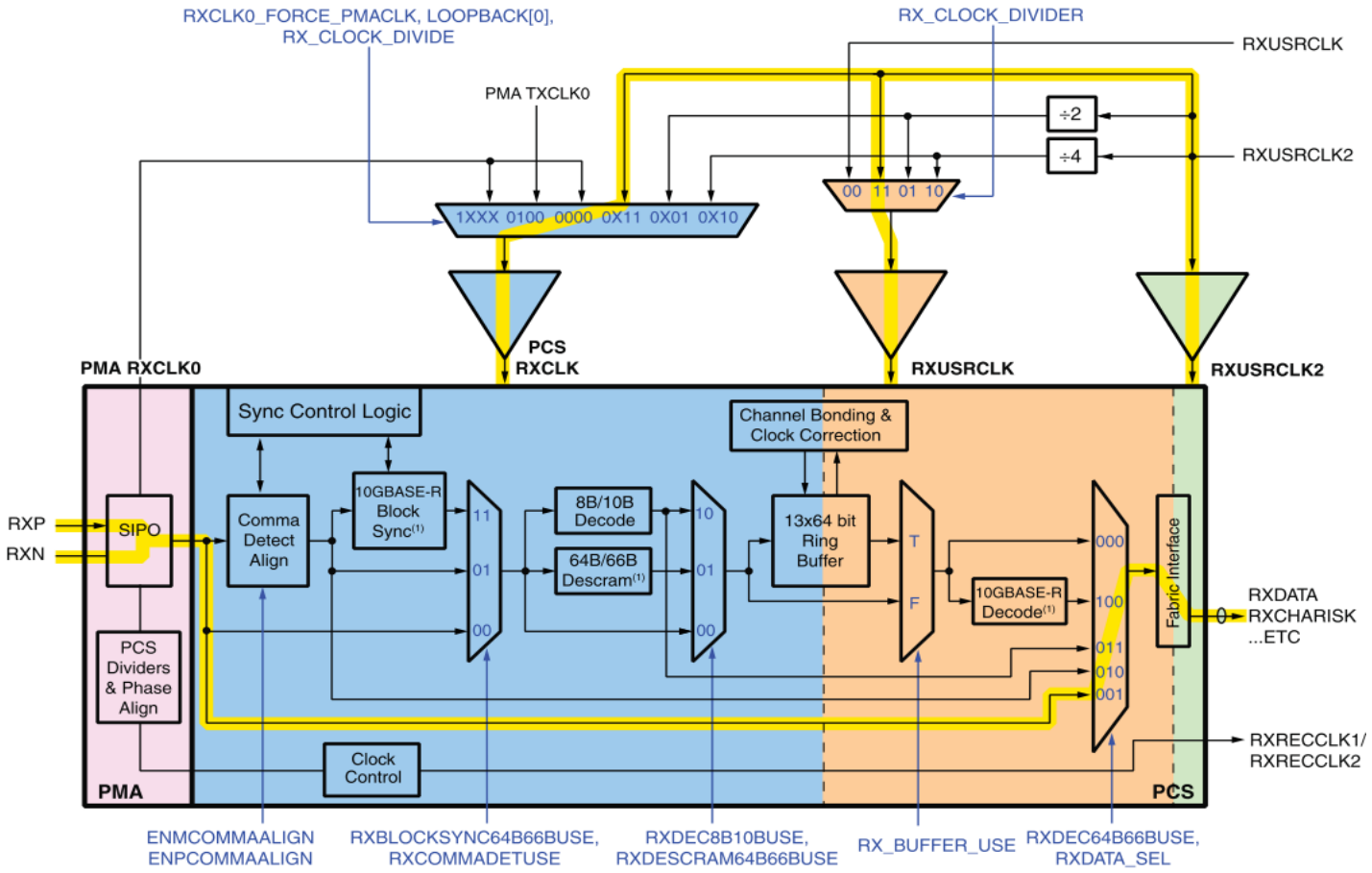
MGT Interface



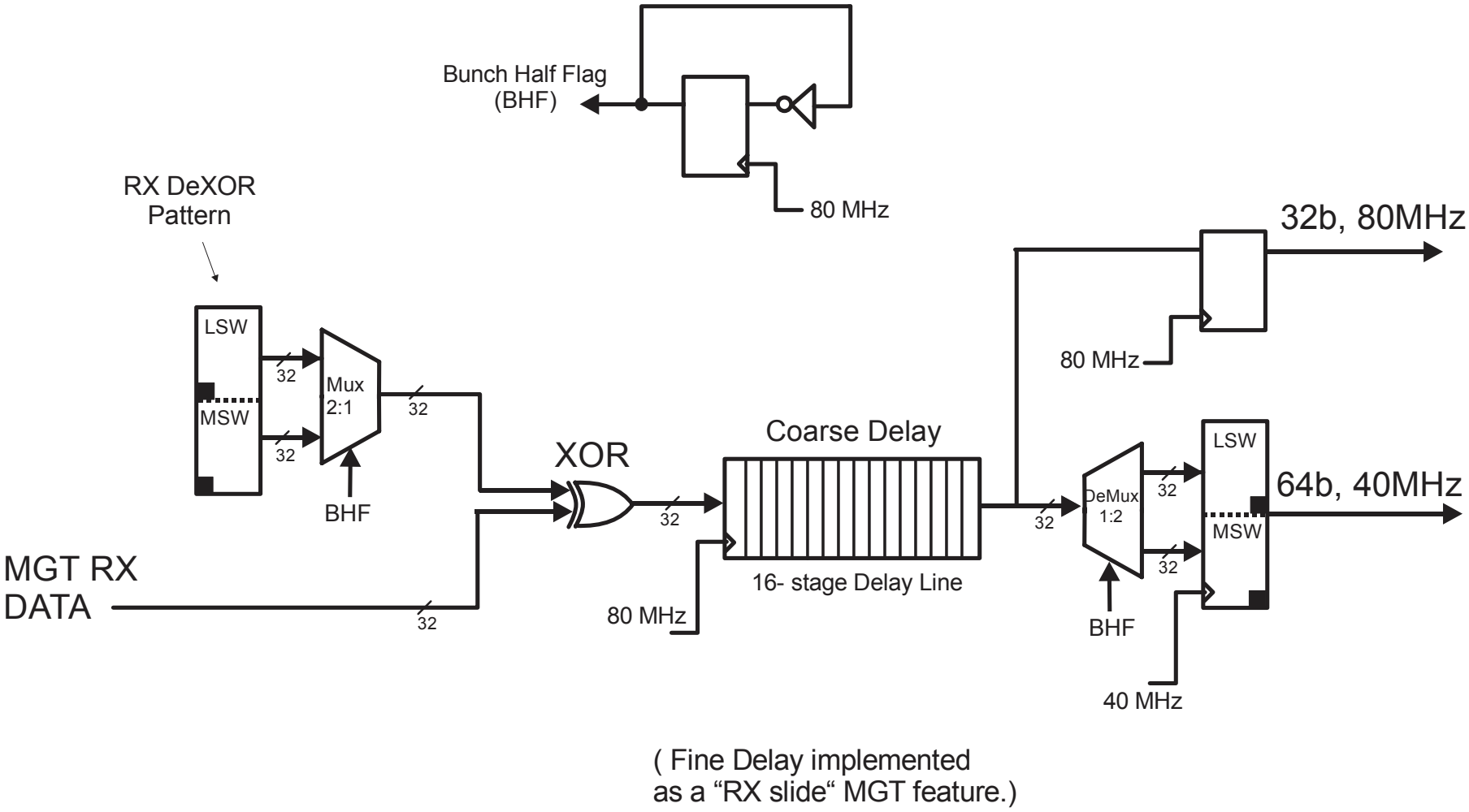
MGT Transmit Path



MGT RX Operating Mode

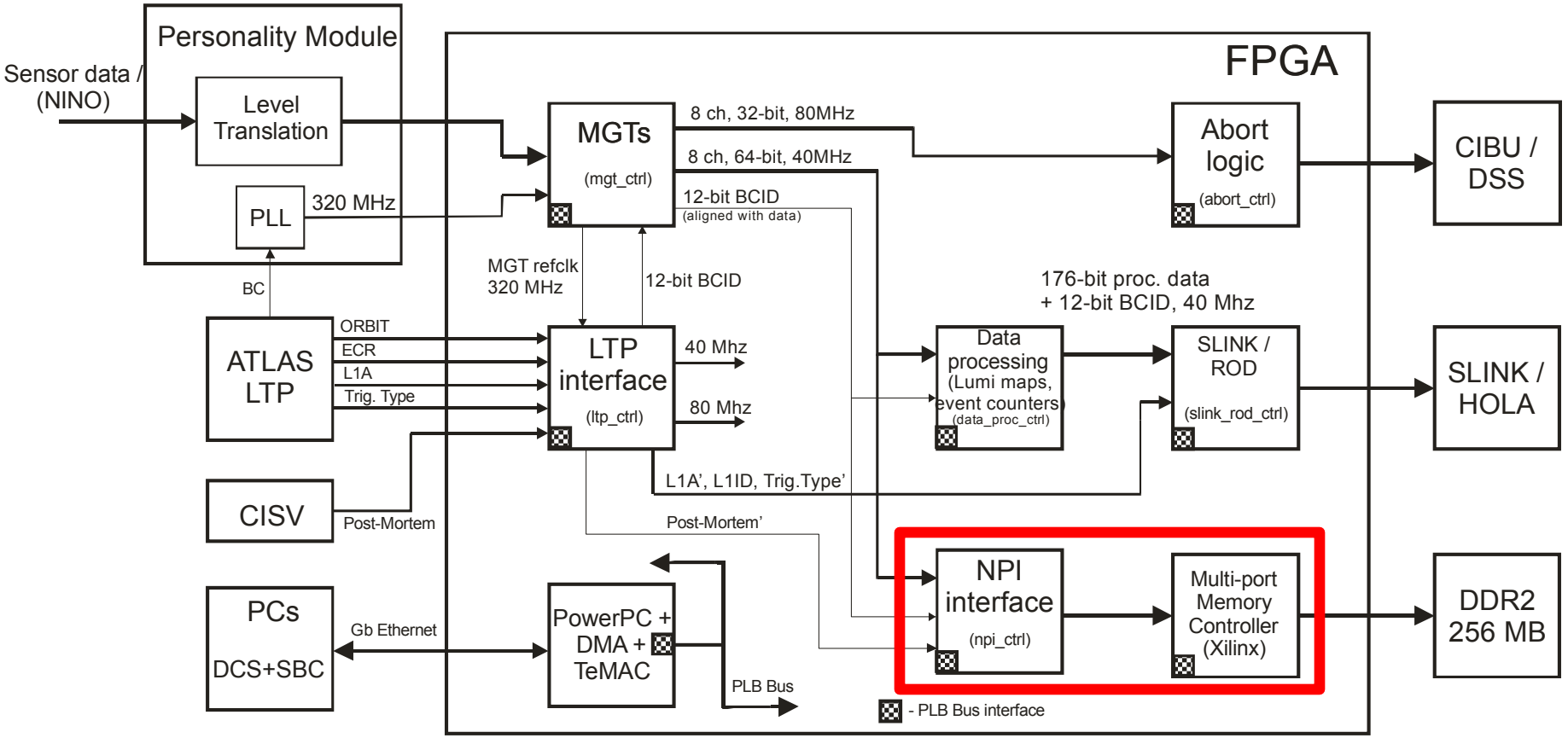


MGT Receive Path



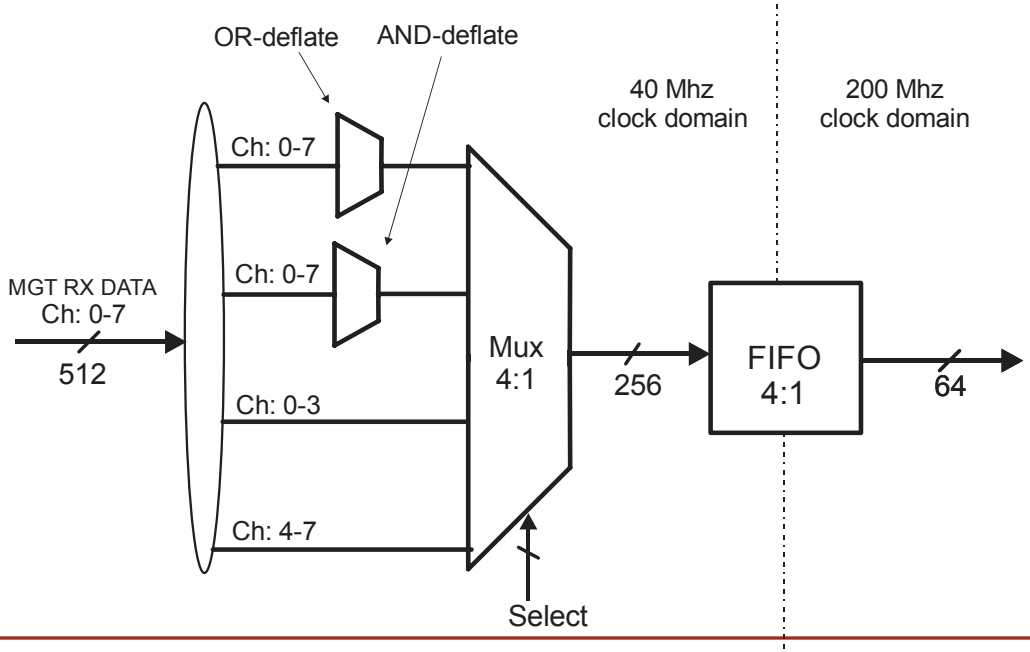
(Fine Delay implemented
as a “RX slide“ MGT feature.)

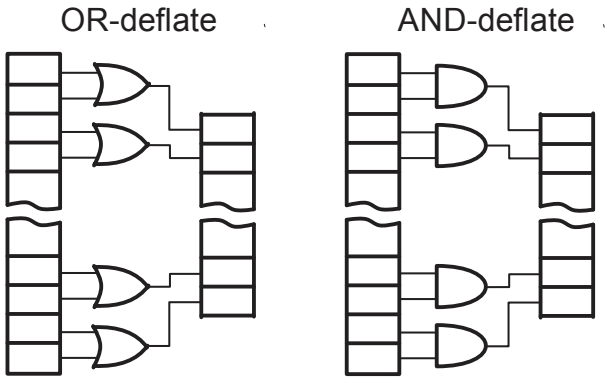
BCM FPGA Data Flow



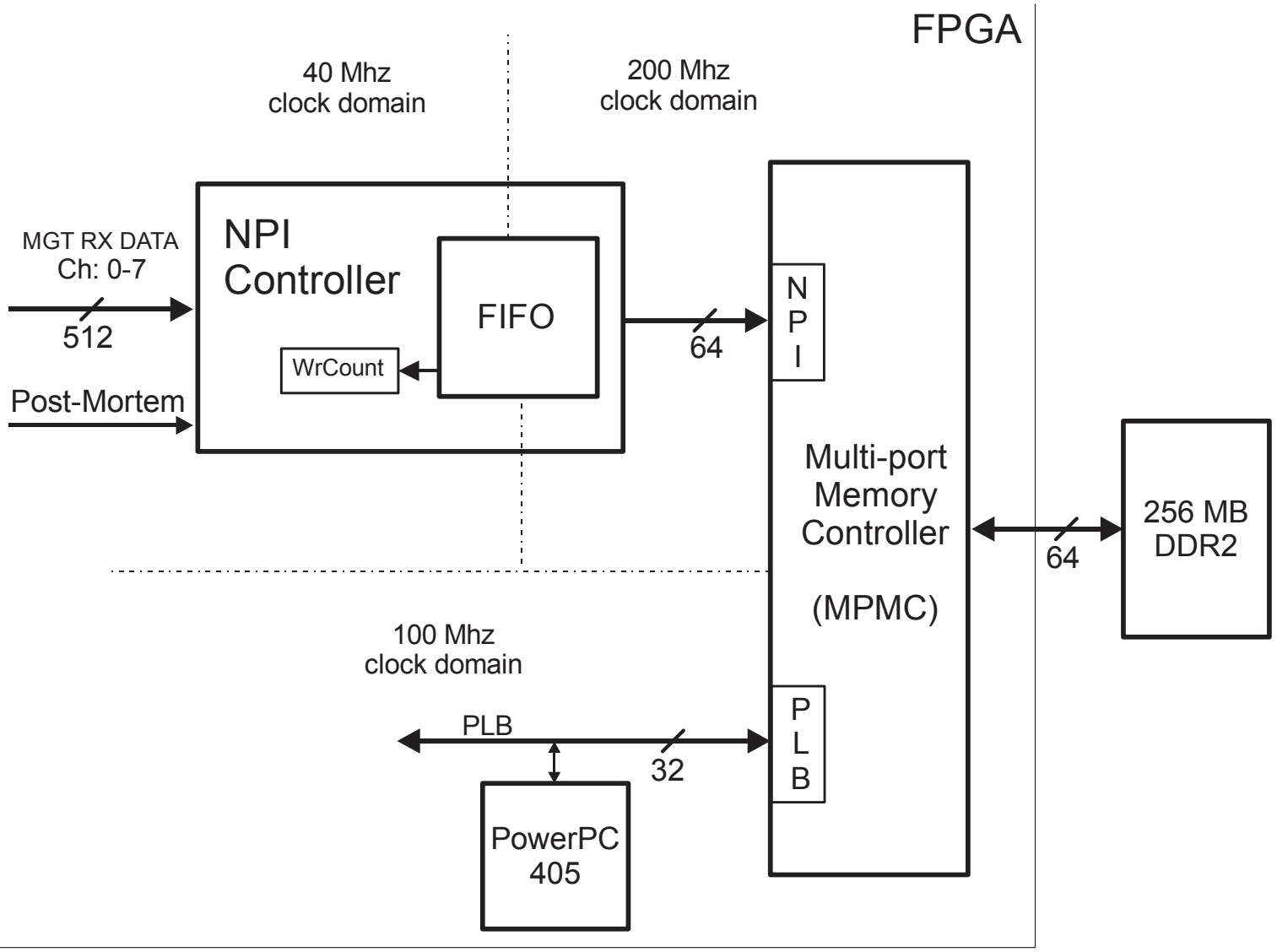
NPI Controller

- Separate 256 MB of DDR2 RAM in 2x128 MB buffers
- Simultaneous read/write ➔ MPMC
- Maximum write speed on 1 MPMC port: 1600 MB/s
- Actual data: 2560 MB/s ➔ reduce the amount of recorded data,reduce resolution from 390 to 780 ps

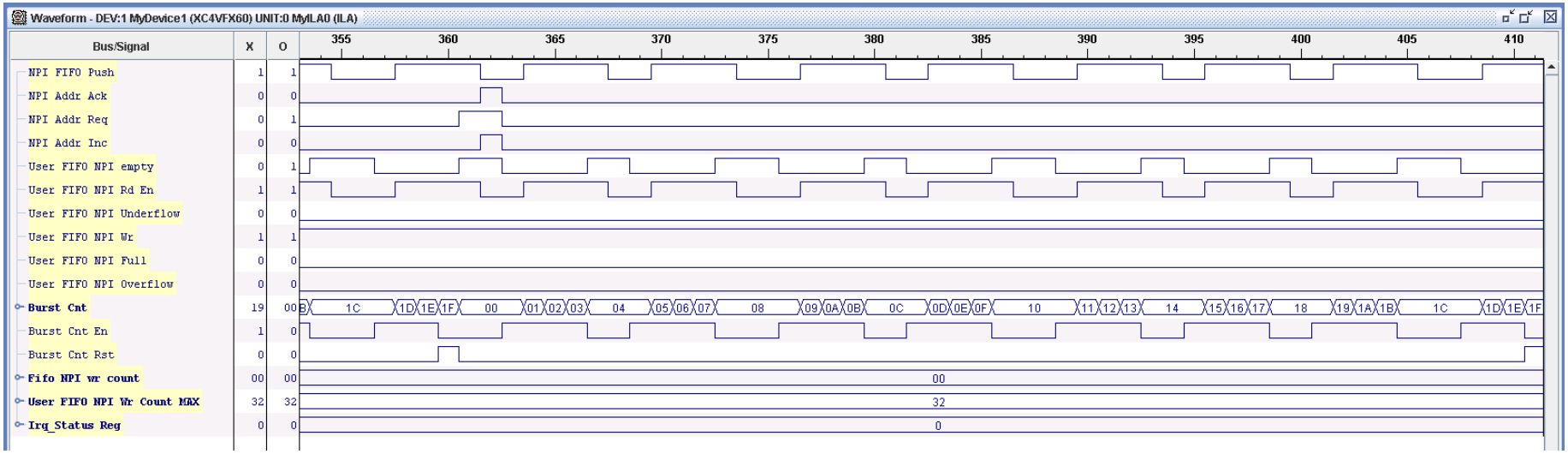




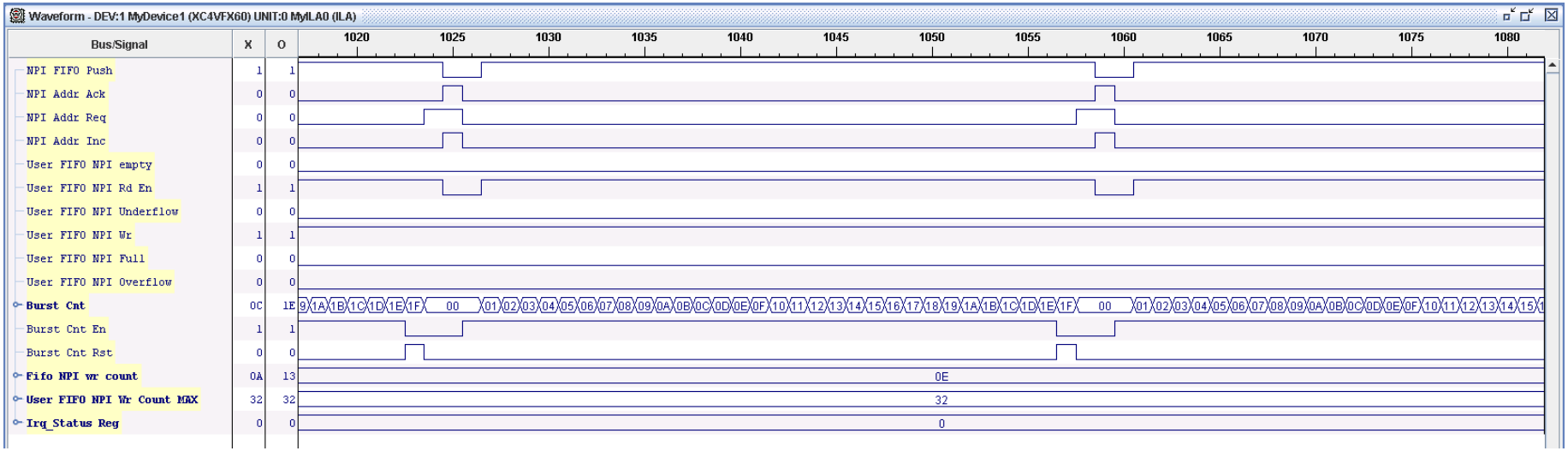
NPI Data Path



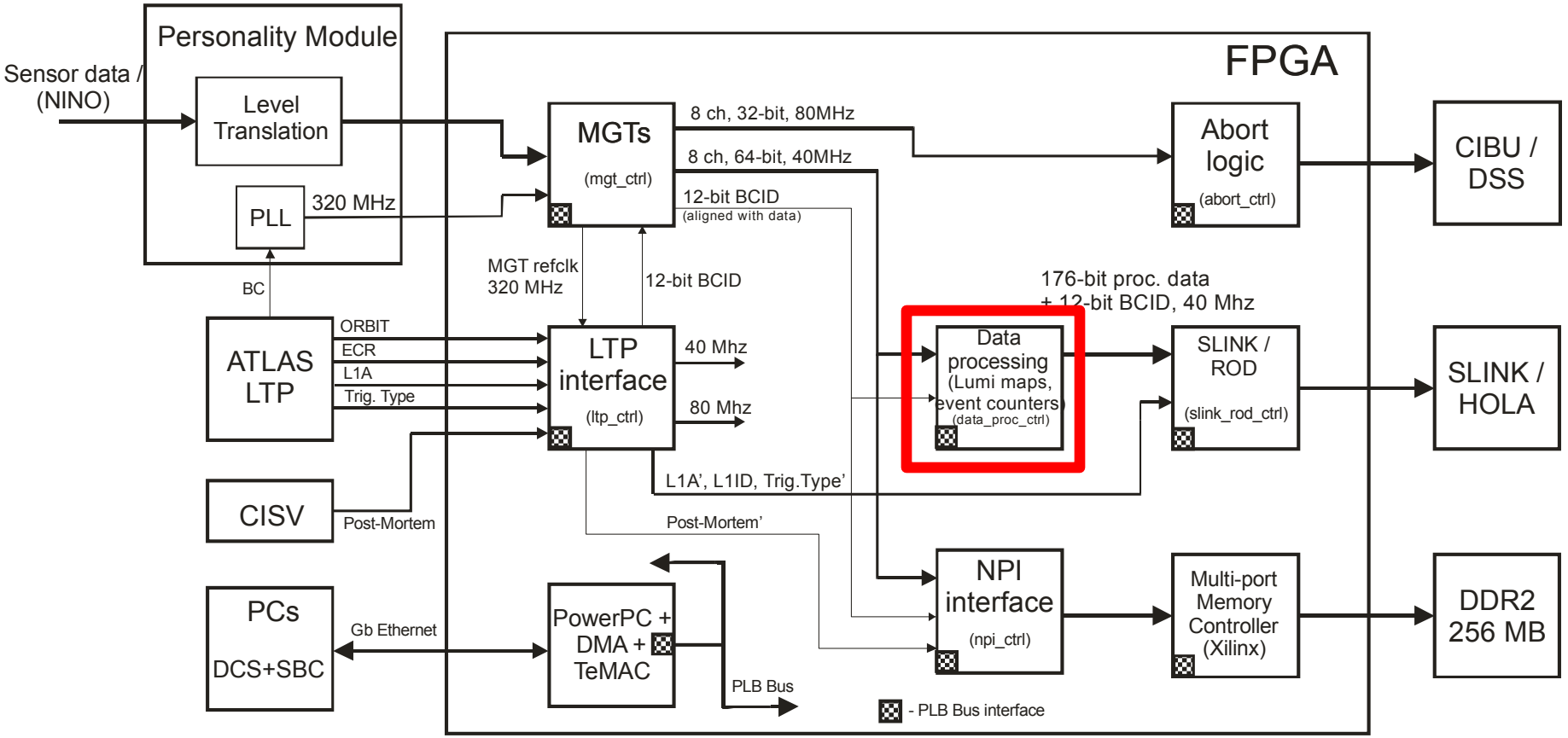
NPI Signaling (FIFO empty)



NPI Signaling (FIFO not empty)



BCM FPGA Data Flow



Data Processing

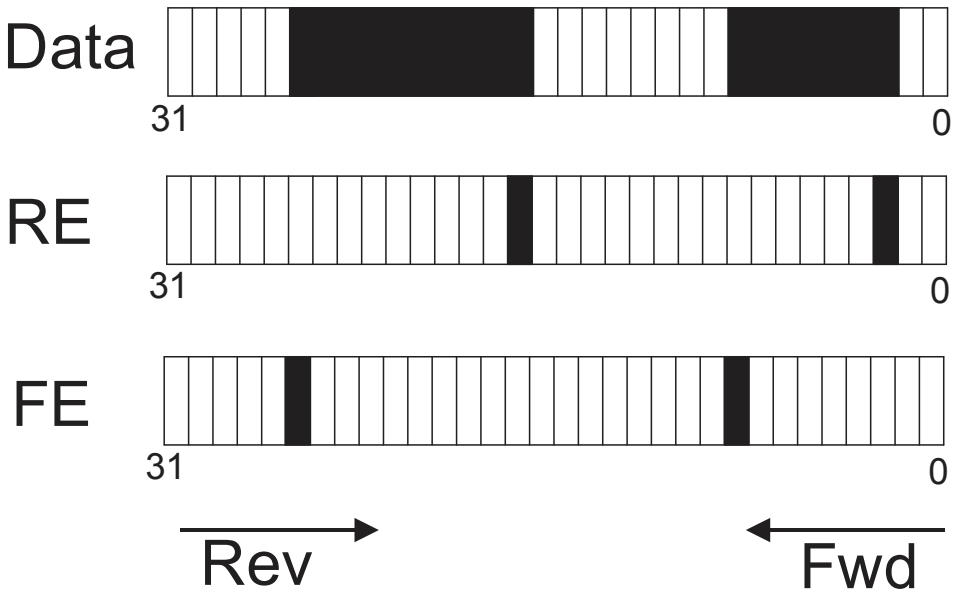
- Based on pulse reconstruction on 64-bit data
- Reconstruct max. 2 pulses in one BC sample
- Count number of pulses (hits)
- Each pulse encoded in:
  - 6-bit rising edge position
  - 5-bit pulse width
- Calculate collisions, background events and lumi conditions by applying time-windows
- Provide 176-bit data stream to TDAQ

  (8 ch × 2 pulses × (6-bit + 5-bit))

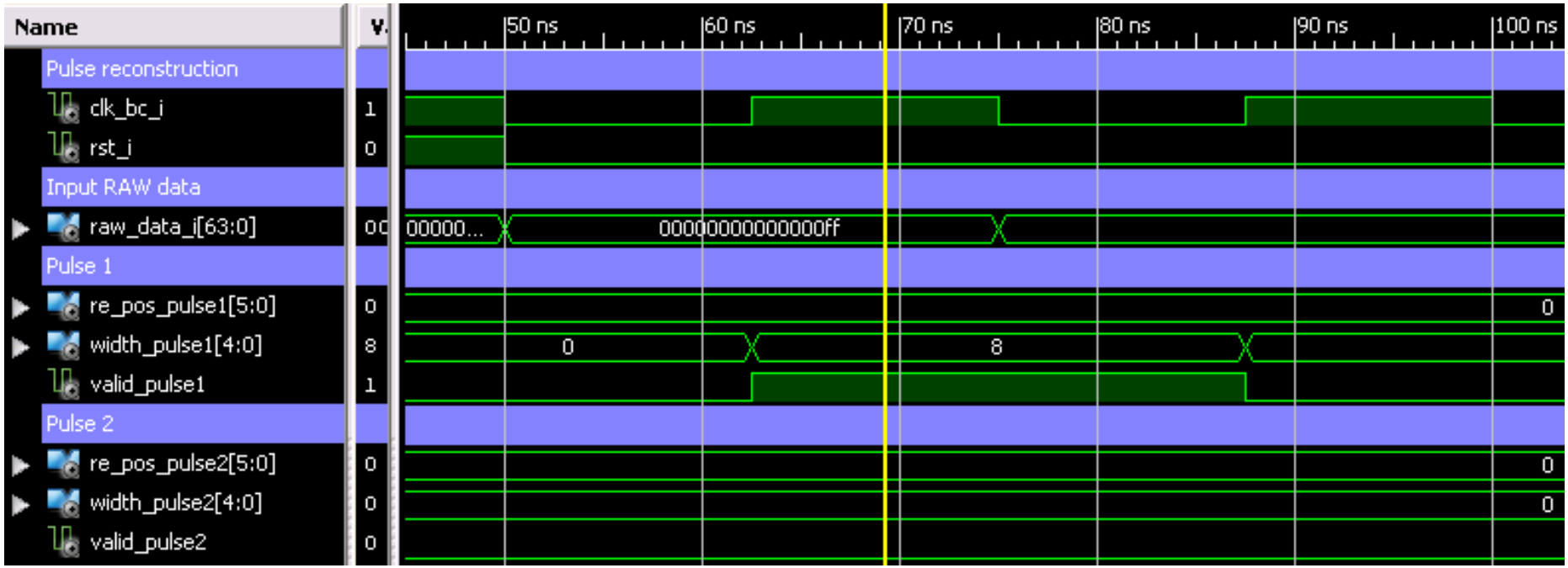
Pulse Reconstruction 1/2

- Calculate rising (RE) and falling(FE) edges in a sample
- Search for first bit set (“1”) from forward (FWD) and reverse (REV) direction on RE and FE ➔
- Pulse 1: position = FWD_RE
  width = FWD_FE – FWD_RE
- Pulse 2: position = REV_RE
  width = REV_FE – REV_RE
- Examples follow

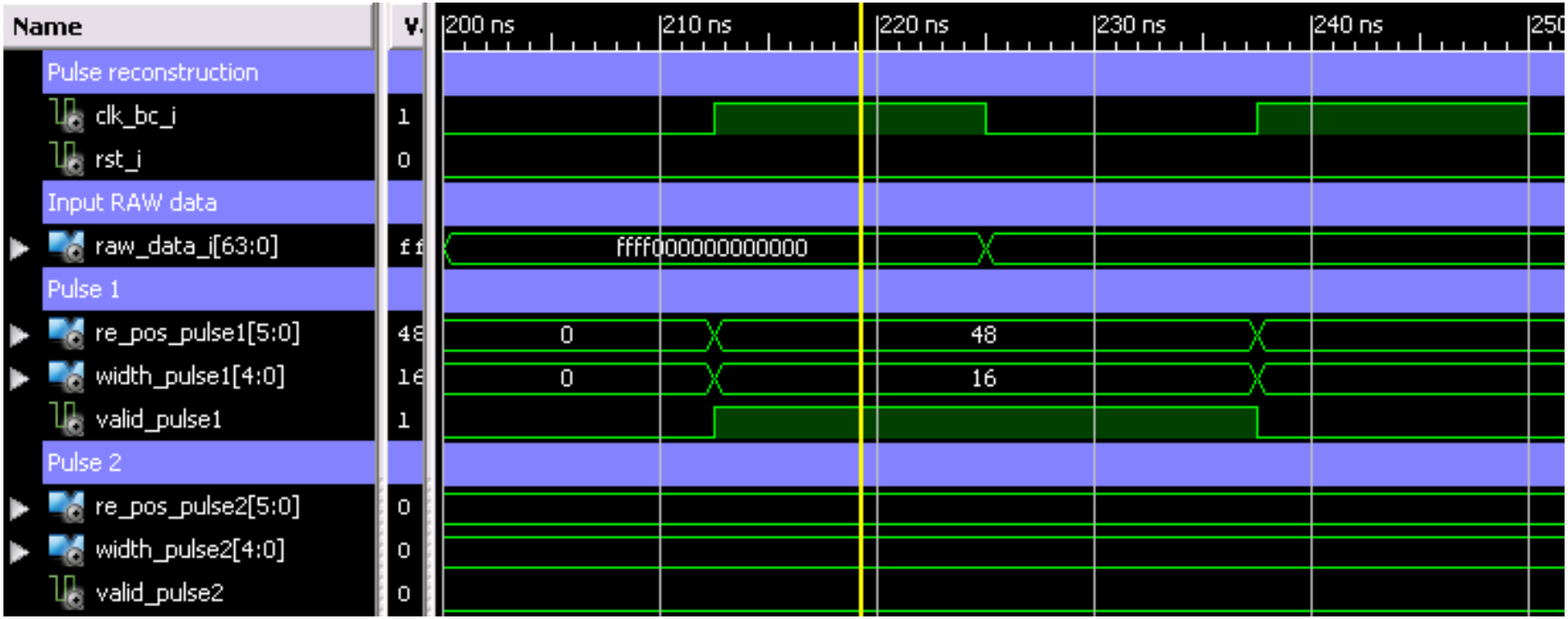
Pulse Reconstruction 2/2



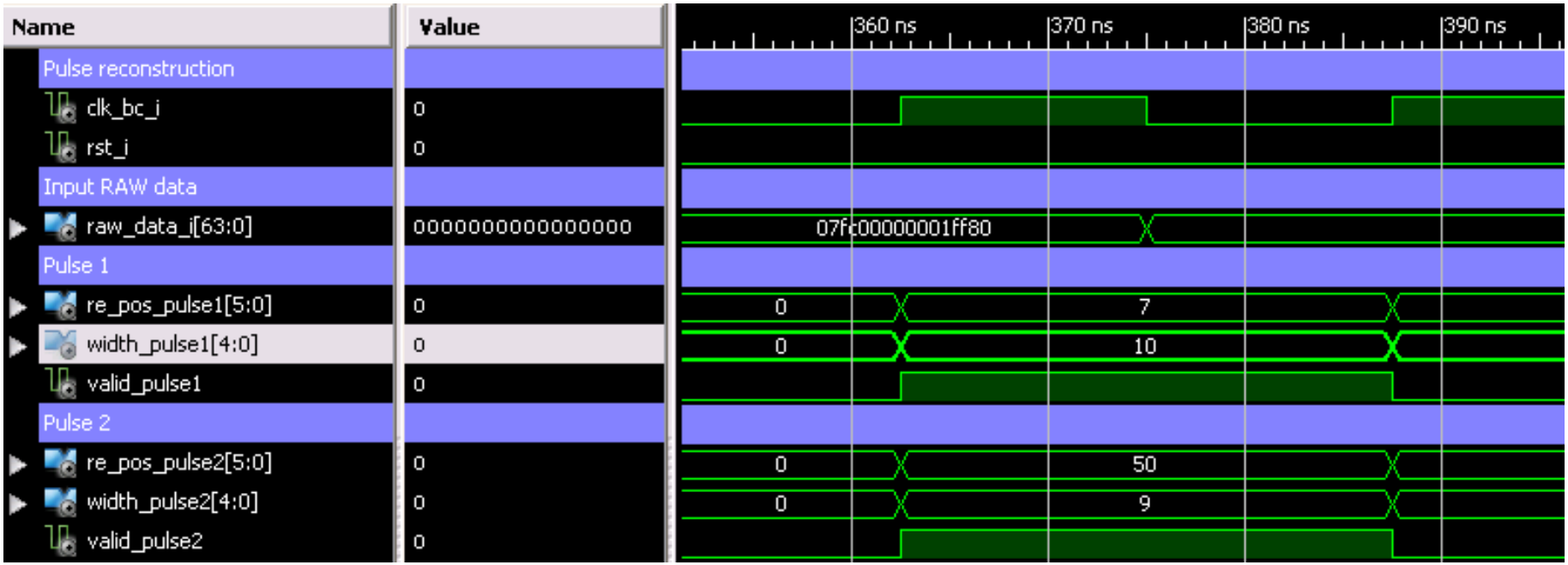
Pulse Reconstruction Simulation



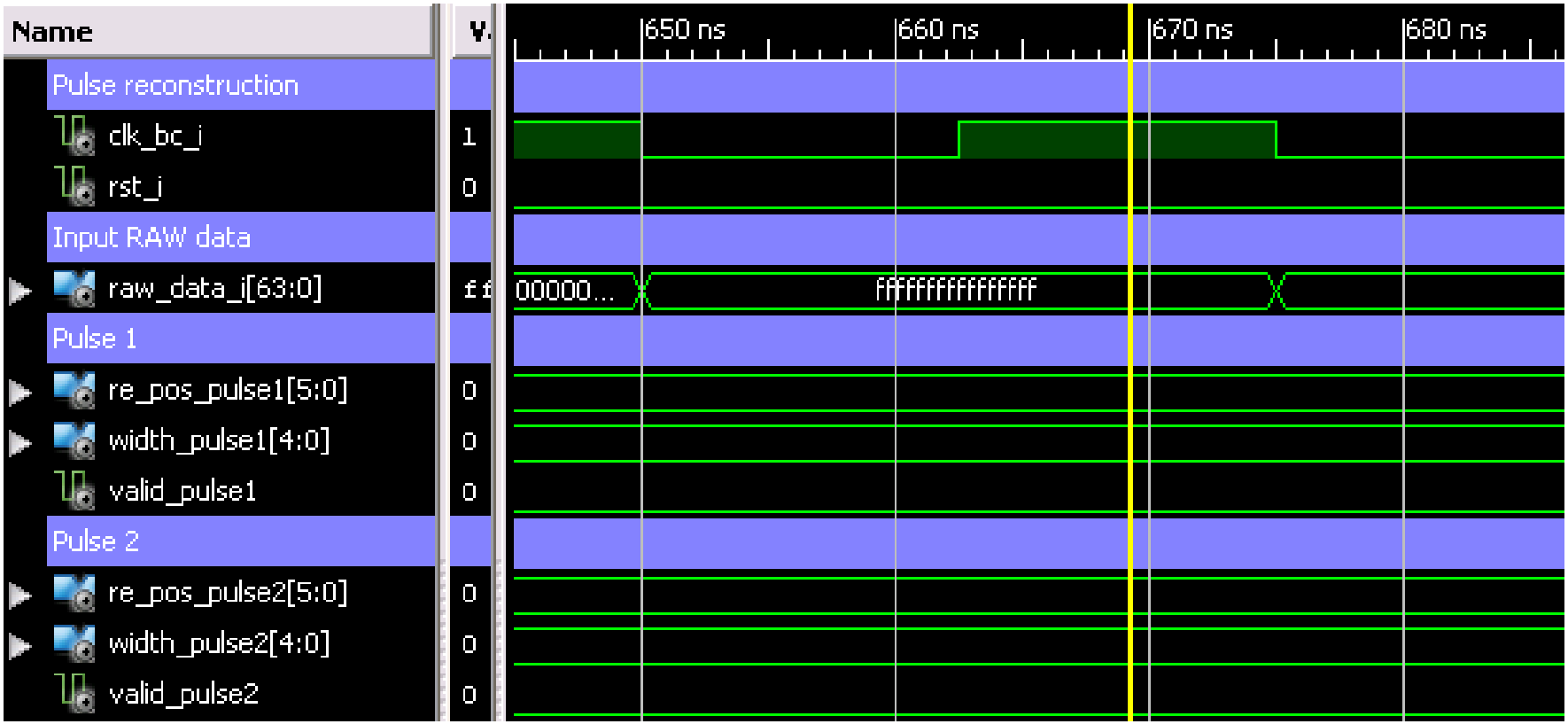
Pulse Reconstruction Simulation



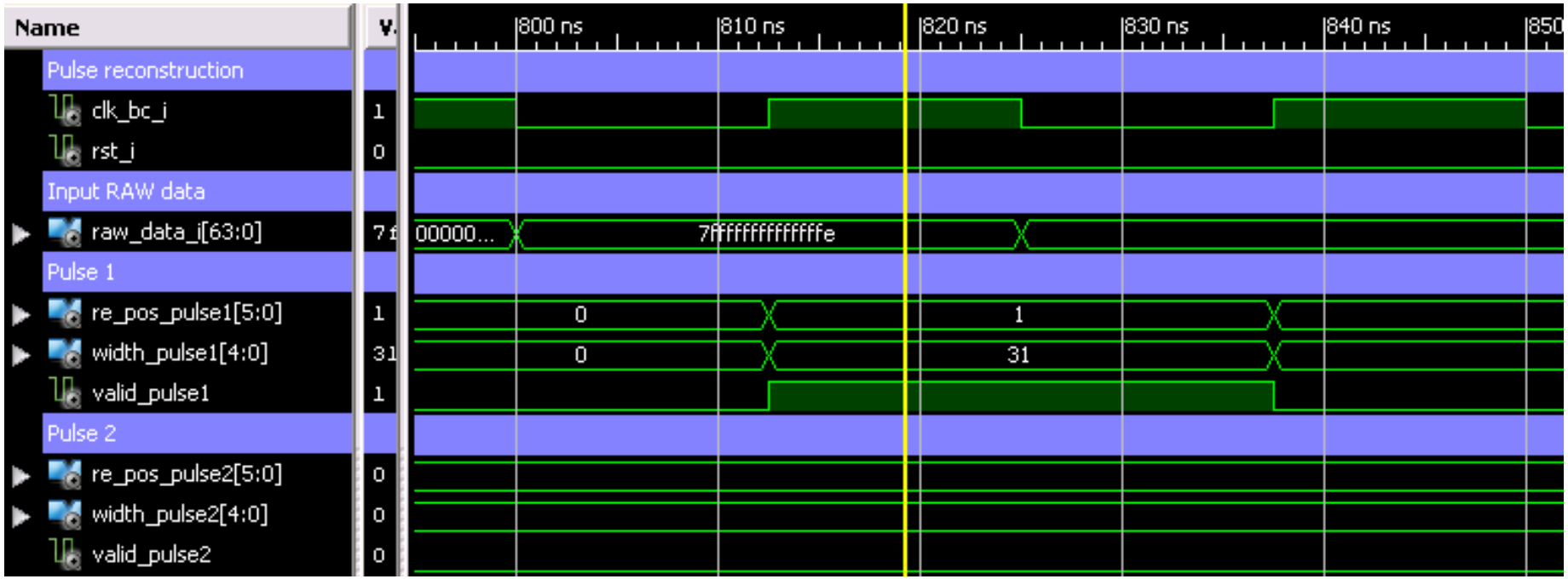
Pulse Reconstruction Simulation



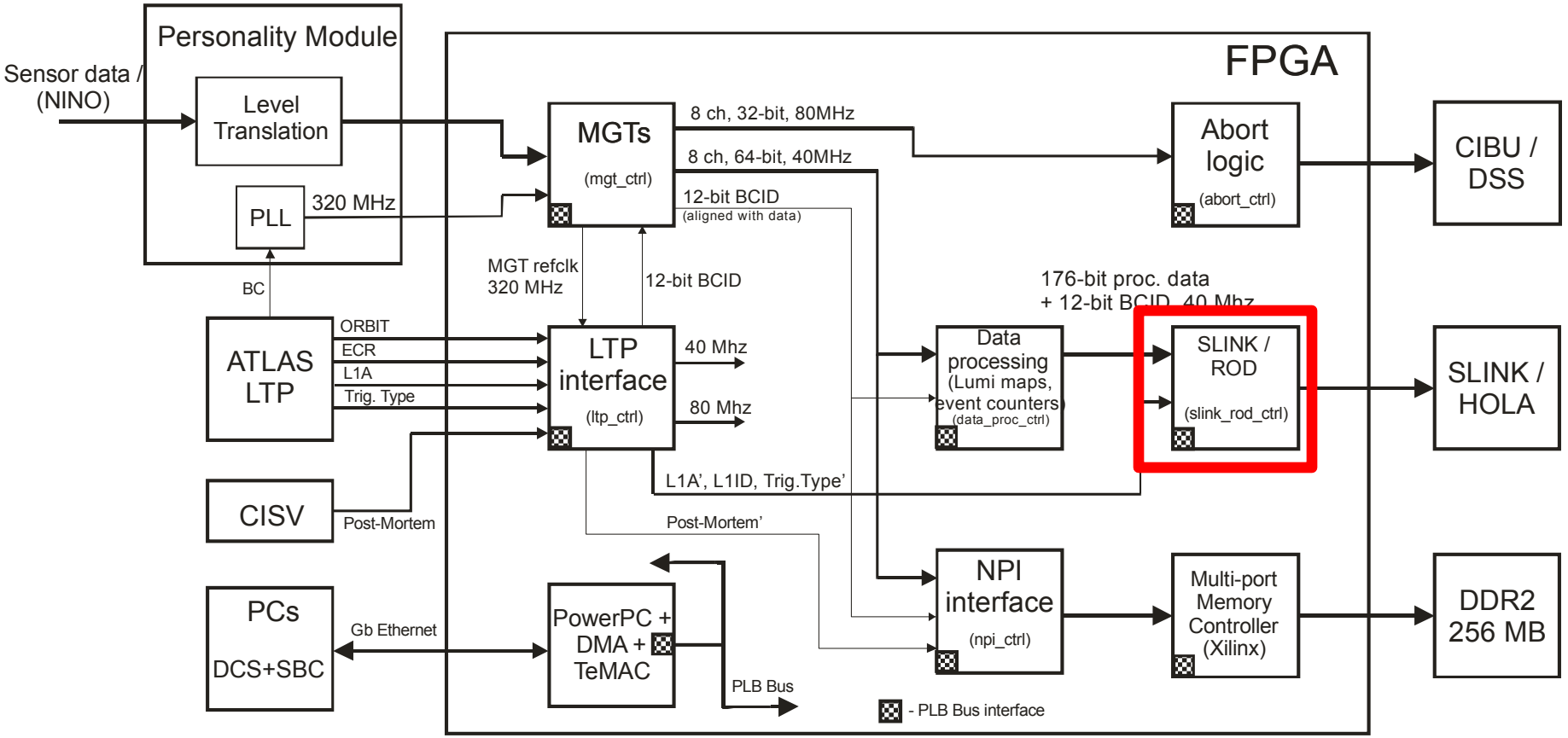
Pulse Reconstruction Simulation



Pulse Reconstruction Simulation



BCM FPGA Data Flow



BCM SLINK/ROD Data Format

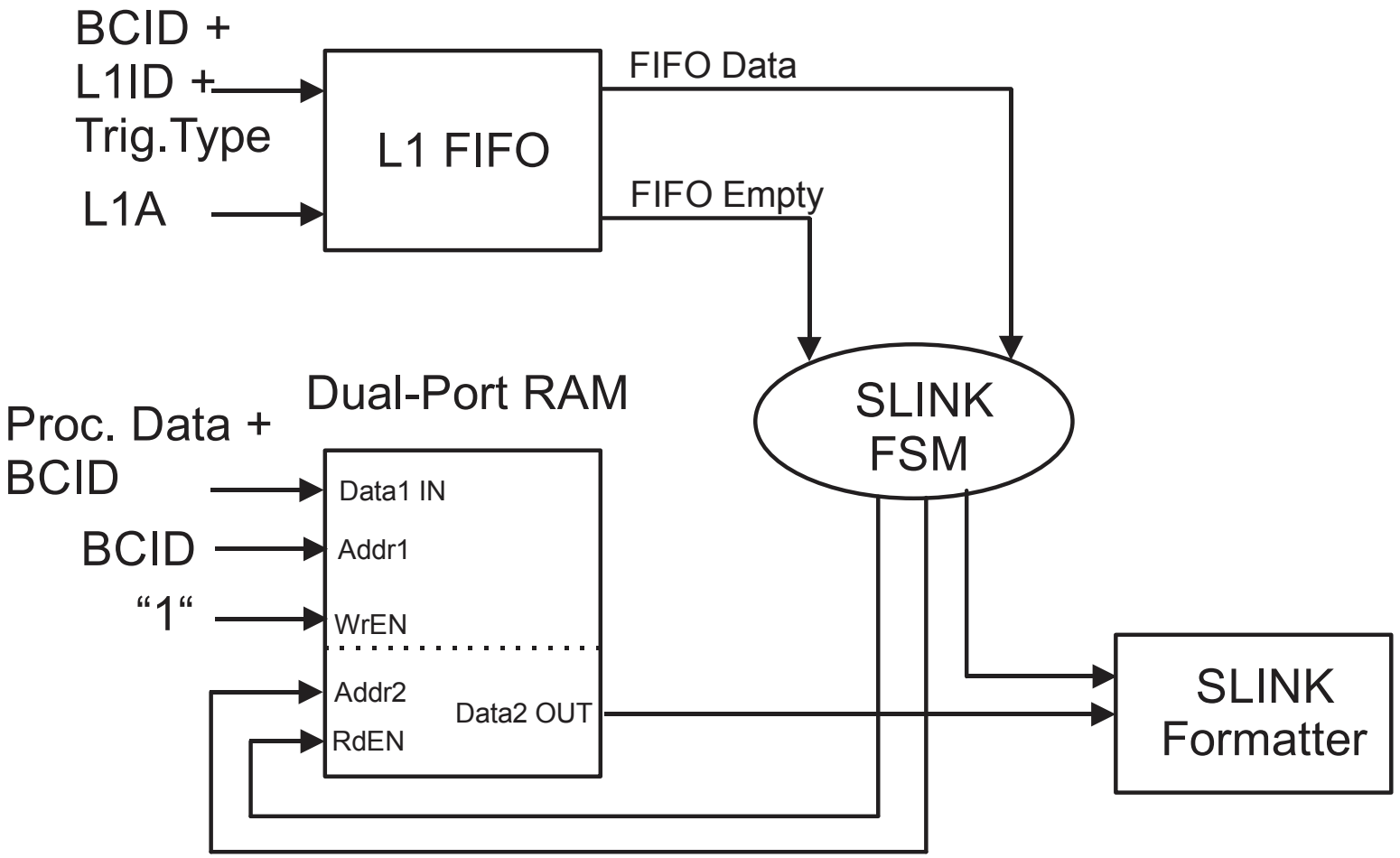
P{1,2}{x,w}[n] refers to pulse 1/2 position/width for channel n.

ROD Section	32-bit Word Counter	Word Description
HEADER	1	Start of ROD header
HEADER	2	Header size
HEADER	3	ROD version
HEADER	4	ROD source ID (see BcmMapping)
HEADER	5	0 + 31-bit run number
HEADER	6	Extended L1ID (24-bit L1ID + 8-bit ECRC)
HEADER	7	0x00000 + 12-bit BCID
HEADER	8	0x000000 + 8-bit Level-1 trigger type
HEADER	9	Detector event type
DATA	1	12-bit BCID + 6-bit P1x[0] + 5-bit P1w[0] + 6-bit P2x[0] + 3-bit P2w[0]
DATA	2	2-bit P2w[0] + 6-bit P1x[1] + 5-bit P1w[1] + 6-bit P2x[1] + 5-bit P2w[1] + 6-bit P1x[2] + 2-bit P1w[2]
DATA	3	3-bit P1w[2] + 6-bit P2x[2] + 5-bit P2w[2] + 6-bit P1x[3] + 5-bit P1w[3] + 6-bit P2x[3] + 1-bit P2w[3]
DATA	4	4-bit P2w[3] + 6-bit P1x[4] + 5-bit P1w[4] + 6-bit P2x[4] + 5-bit P2w[4] + 6-bit P1x[5]
DATA	5	5-bit P1w[5] + 6-bit P2x[5] + 5-bit P2w[5] + 6-bit P1x[6] + 5-bit P1w[6] + 5-bit P2x[6]
DATA	6	1-bit P2x[6] + 5-bit P2w[6] + 6-bit P1x[7] + 5-bit P1w[7] + 6-bit P2x[7] + 5-bit P2w[7] + 4-bit Error code
TRAILER	1	Status word 1 - bit errors
TRAILER	2	Status word 2 - count of words with errors
TRAILER	3	Number of status words
TRAILER	4	Number of data words
TRAILER	5	Status block position (0=bef,1=aft data words)

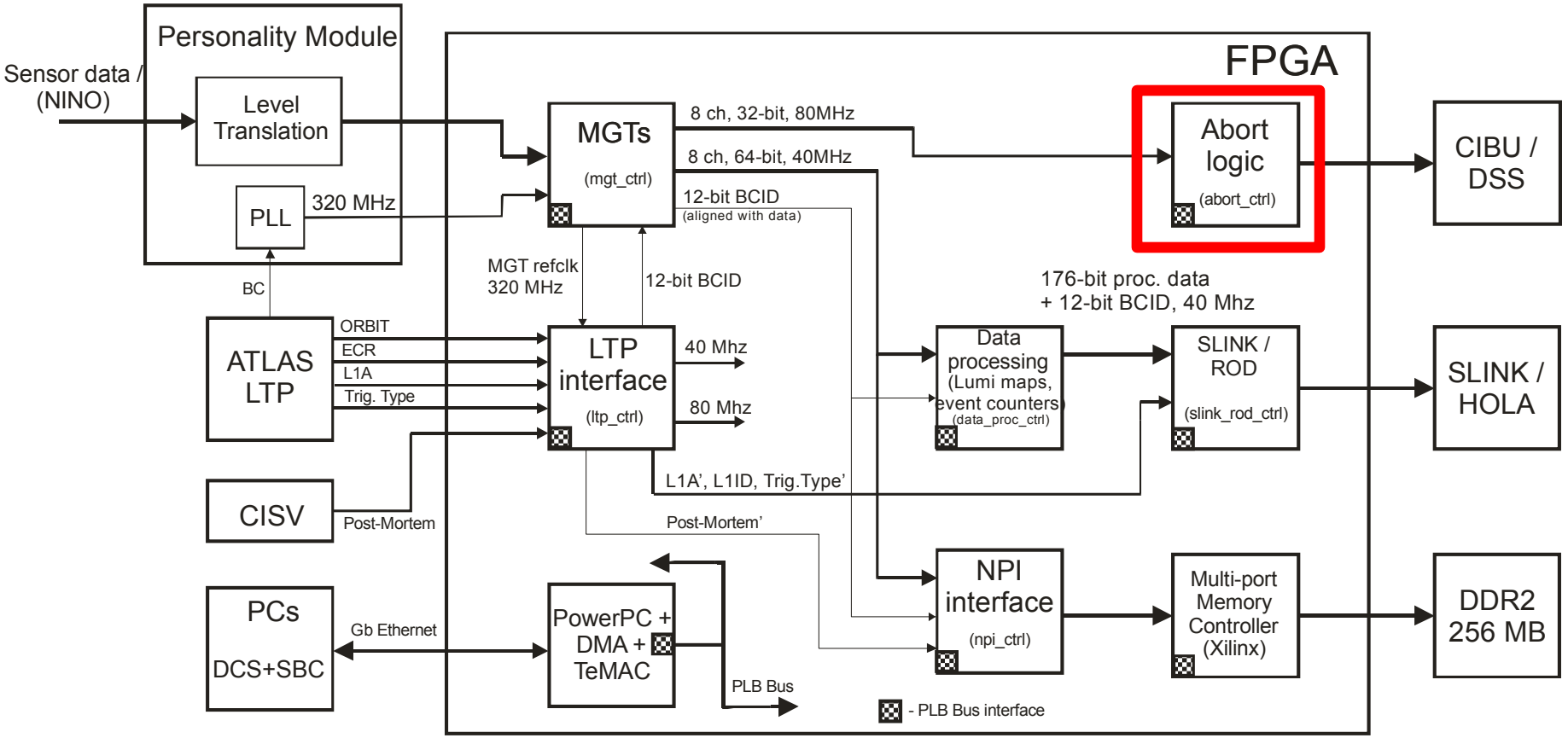
12-bit BCID
+ 176-bit of data
+ 4-bit error code
per BC

https://twiki.cern.ch/twiki/bin/view/Atlas/BcmRod

SLINK ROD Controller



BCM FPGA Data Flow

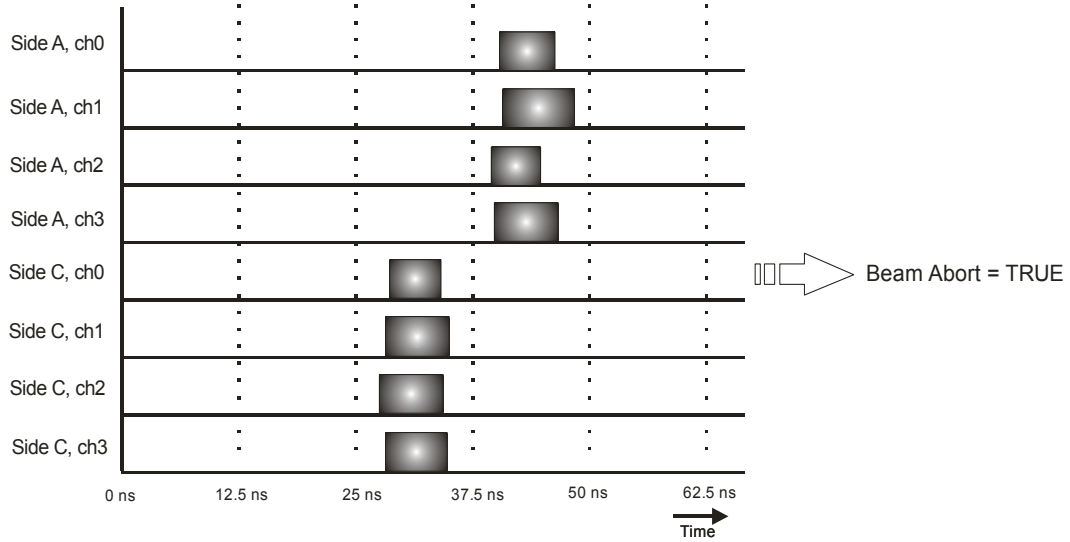


Abort Logic

- Search for background pattern
- The same pulse reconstruction logic, but 32-bit data @ 80 MHz
- cond3_sideX = at least 3 out of 4 valid pulses at side X

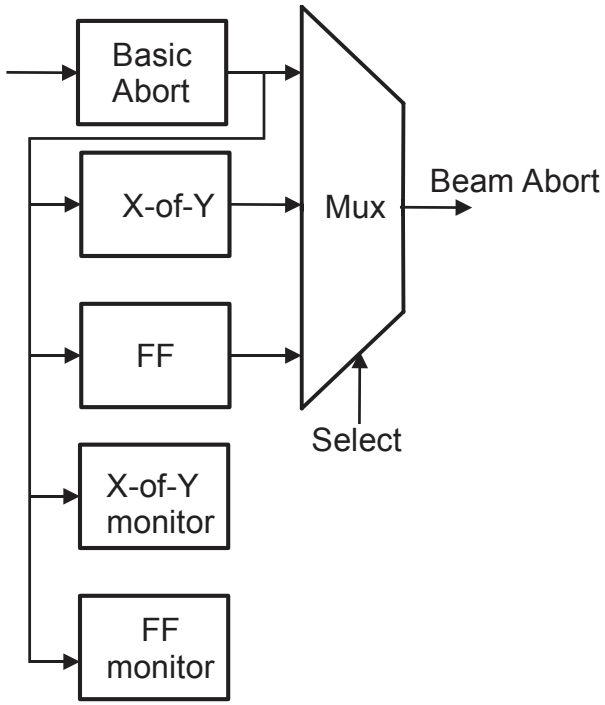
Basic Abort:

```
If  (cond3_sideA AND cond3_sideC_dly )  OR
    (cond3_sideC AND cond3_sideA_dly )))
      BA = ACTIVE
Else
      BA = NOT ACTIVE
```

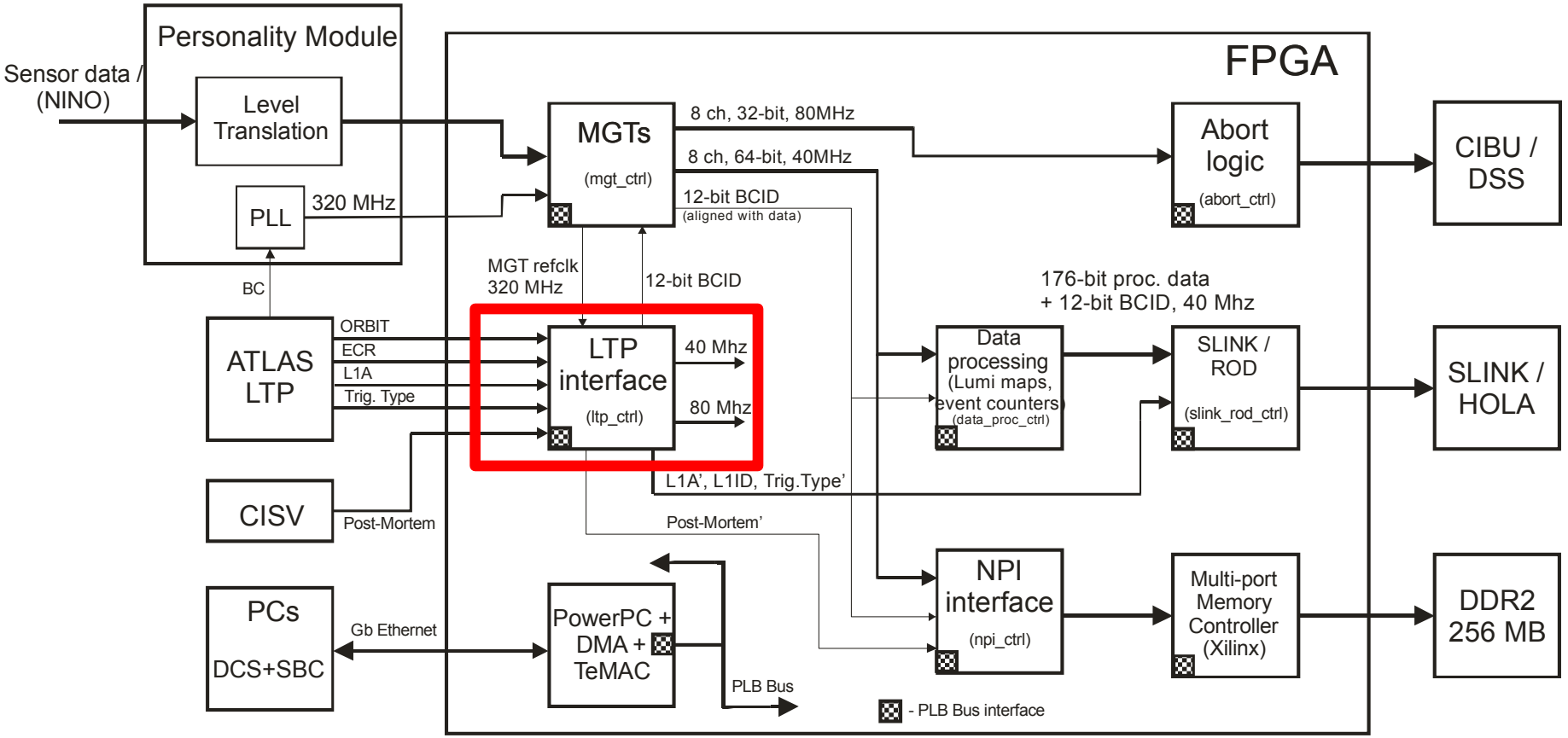


Additional Abort Algorithms

- **Basic Beam Abort** (desribed on previous slide)
- **X-of-Y** : takes into account last Y Basic Abort results and demands that at least X of them will fire before it issues an abort condition.
- **Forgetting Factor** (Leaky bucket) Extension of Basic Abort algorithm. It provides a more dynamic behaviour by "forgetting« past results as they get older.



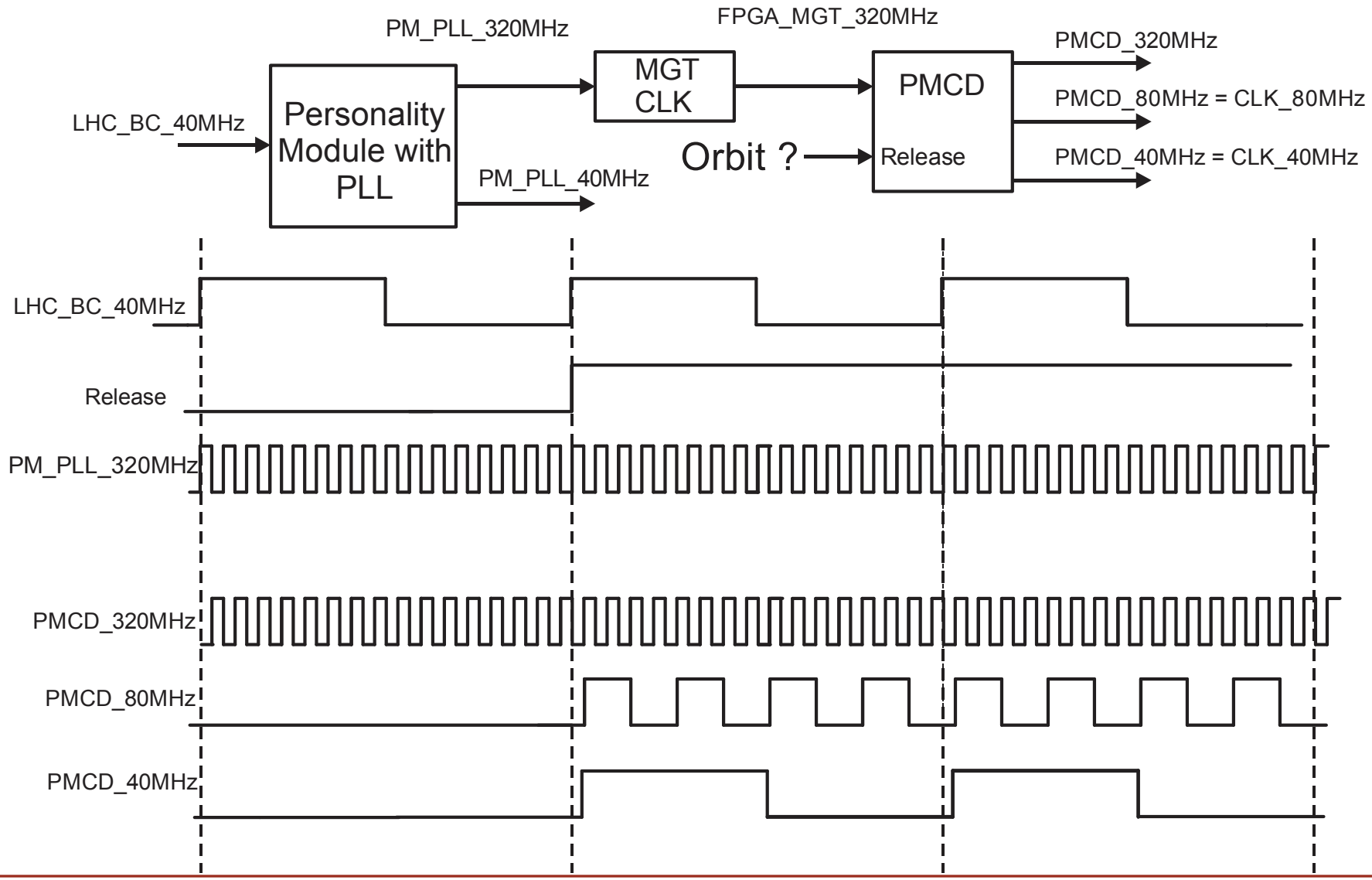
BCM FPGA Data Flow



LTP Controller

- L1ID bookkeeping with ECR load support
- BCID bookkeeping
- Post-Mortem delay
- Regenerate 40 MHz (BC) and 80 MHz from 320 MHz (or use 40 MHz available on the new Personality Modules)
- LTP interface, proper latching of LTP signals (*L1A, ECR, Orbit, Trigger Type*)

40/80 MHz BC Clock Scheme



Xilinx Phase-Matched Clock Divider

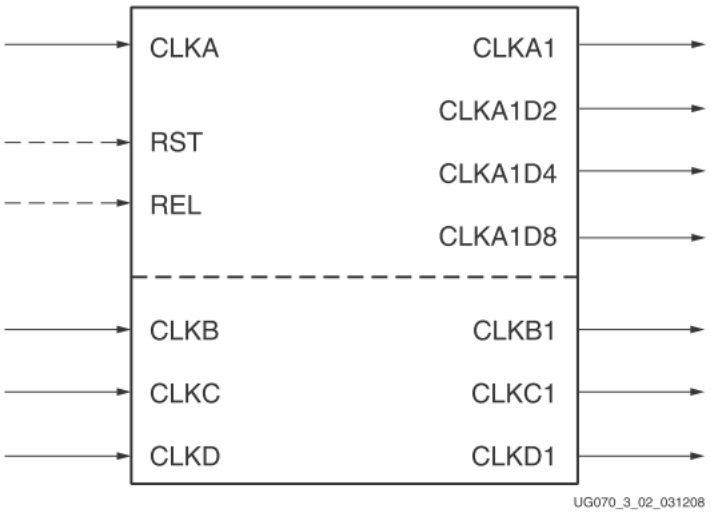


Figure 3-2: **PMCD Primitive**

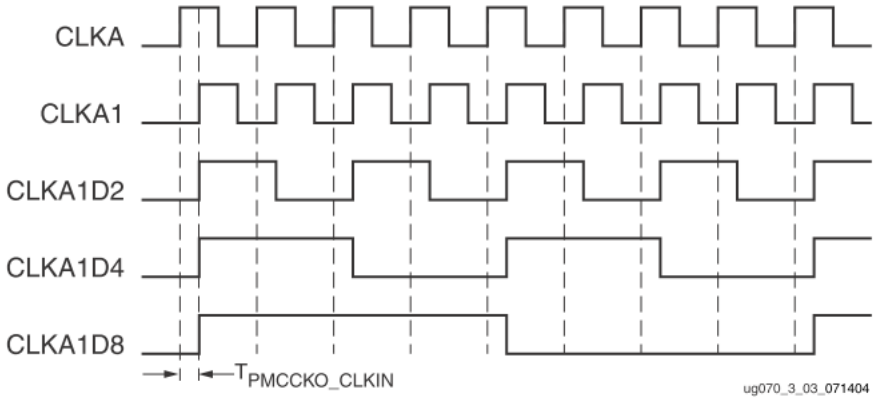


Figure 3-3: **PMCD Frequency Divider**

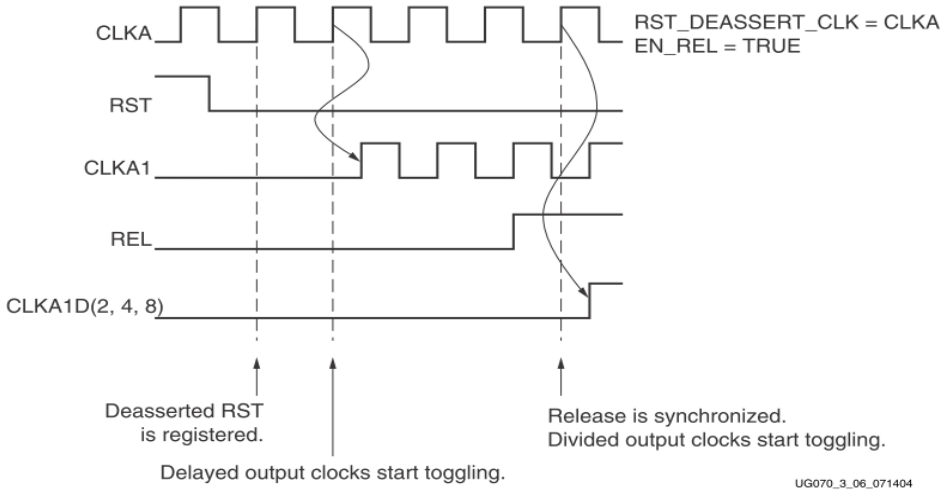
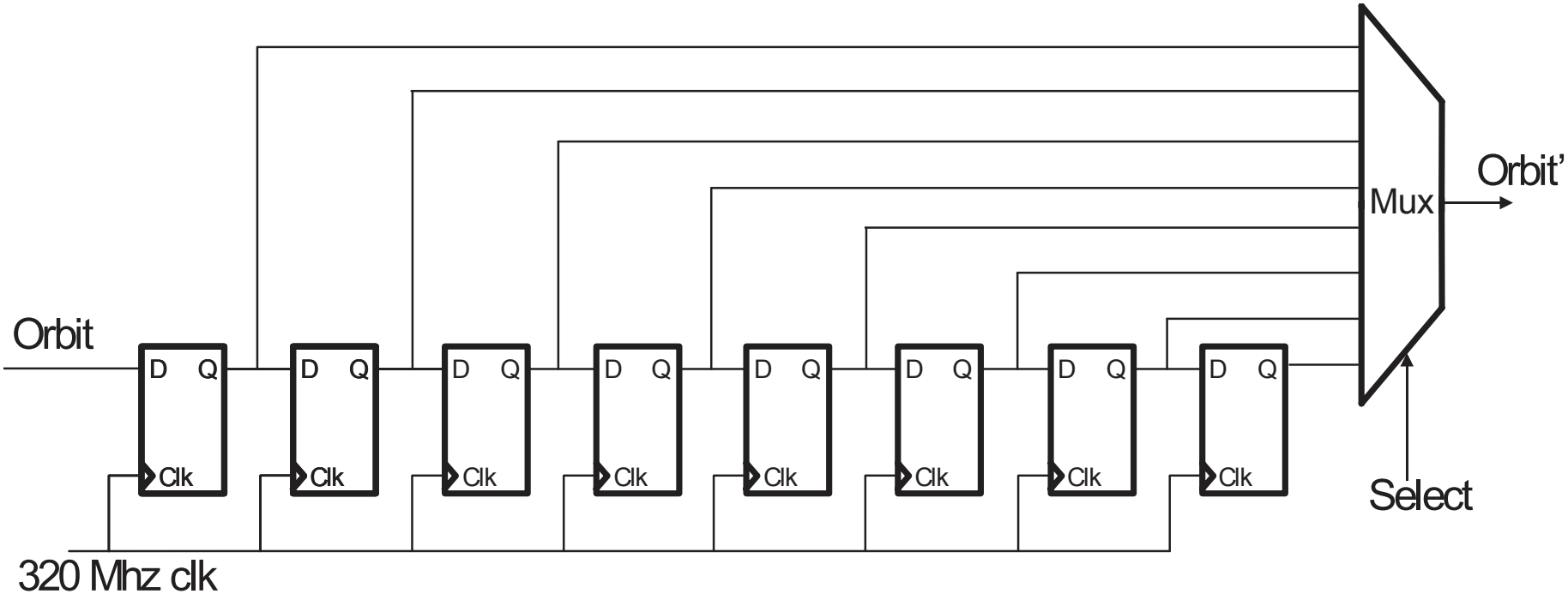


Figure 3-6: **REL Waveform Example**

Orbit Signal Aligning



Device Utilization Summary

Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	20,797	50,560	41%
Number of 4 input LUTs	28,465	50,560	56%
Number of occupied Slices	**21,611**	**25,280**	**85%**
Number of bonded IPADs	24	80	30%
Number of bonded OPADs	18	32	56%
Number of bonded IOBs	222	576	38%
Number of BUFG/BUFGCTRLs	14	32	43%
Number of FIFO16/RAMB16s	**137**	**232**	**59%**
Number of DCM_ADVs	4	12	33%
Number of PMCDs	1	8	12%
Number of PPC405_ADVs	2	2	100%
Number of EMACs	1	2	50%
Number of BUFRs	1	32	3%
Number of JTAGPPCs	1	1	100%
Number of IDELAYCTRLs	10	20	50%
Number of GT11s	10	16	62%
Number of GT11CLKs	2	8	25%
Number of RPM macros	72		
Average Fanout of Non-Clock Nets	3.23		

Module Resource Utilization Breakdown

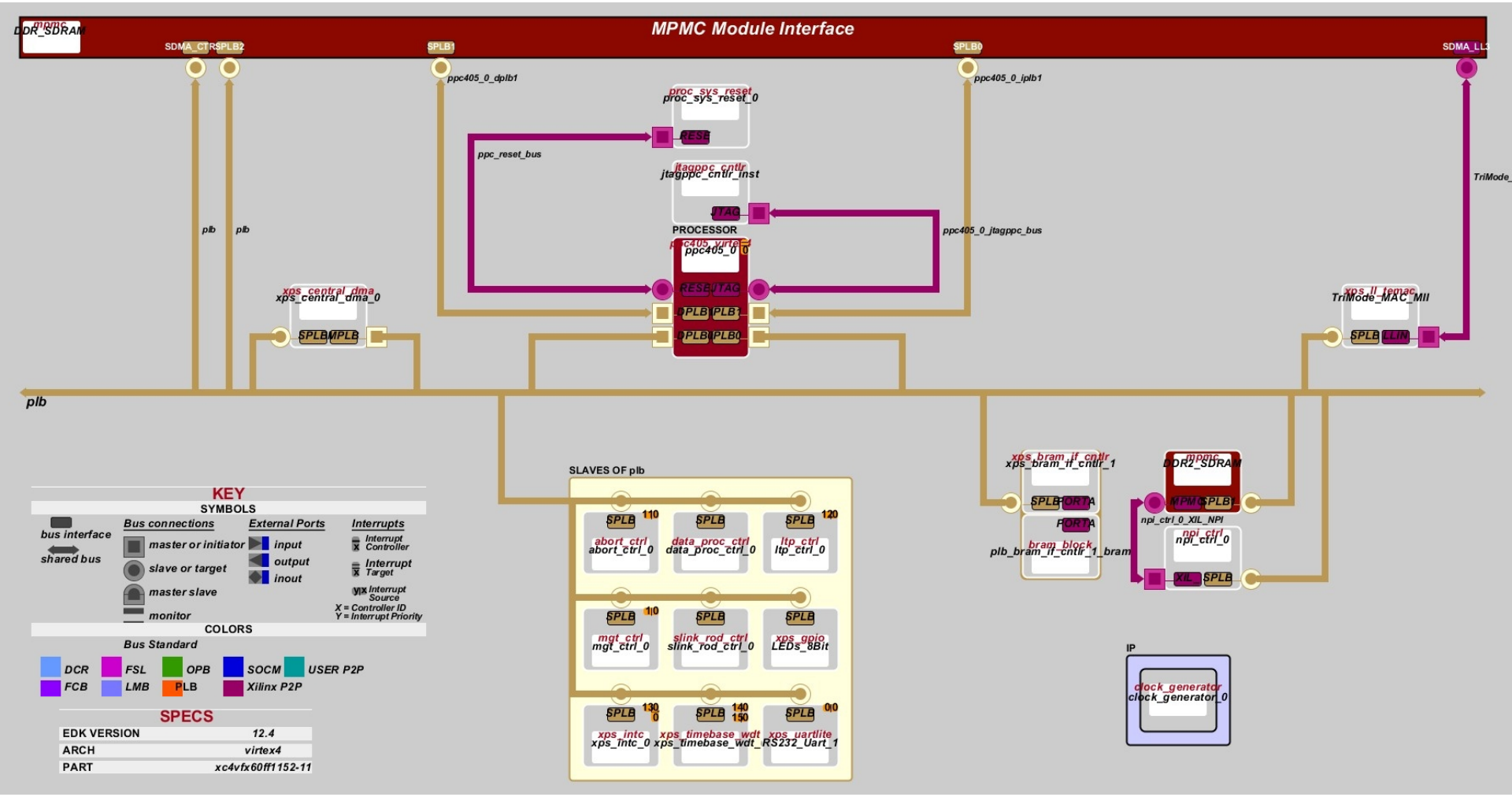
XPS Synthesis Summary Report *	Flip Flops Used	LUTs Used
proc_system	21715	30401
ddr_sdram_wrapper	**5620**	**6400**
ddr2_sdram_wrapper	3857	3104
trimode_mac_mii_wrapper	**3712**	**3206**
mgt_ctrl_0_wrapper	3405	3073
abort_ctrl_0_wrapper	1392	2626
data_proc_ctrl_0_wrapper	899	5976
npi_ctrl_0_wrapper	711	1177
slink_rod_ctrl_0_wrapper	700	1073
ltp_ctrl_0_wrapper	655	603
xps_central_dma_0_wrapper	**566**	**1005**
ppc405_0_wrapper	381	409
xps_intc_0_wrapper	283	274
xps_bram_if_cntlr_1_wrapper	229	184
plb_wrapper	180	1034
xps_timebase_wdt_0_wrapper	169	224
rs232_uart_1_wrapper	148	143
leds_8bit_wrapper	128	97
proc_sys_reset_0_wrapper	69	54

* XPS Synthesis Summary produces approximate report, but it is still relevant to determine relative size of the modules.

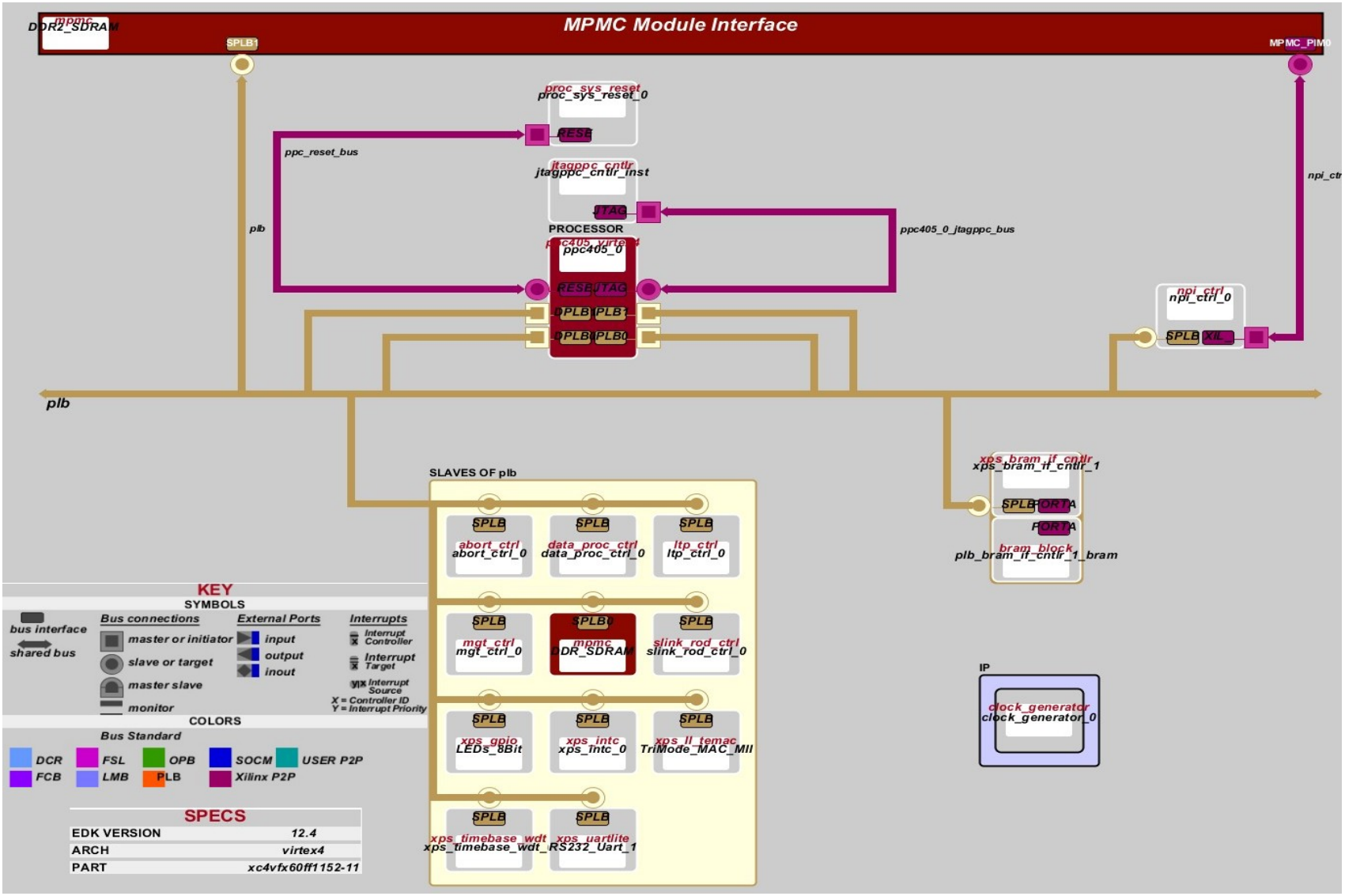
Resource Optimization Strategies

- Optimization will be applied if necessary
- Trade Ethernet speed for FPGA resources
- Processor System Architecture Redesign
- More than 20% of resources can be saved by:
  - reducing DDR 64 MB MPMC to one port
  - excluding DMA controller
  - excluding Ethernet Checksum HW offloading
- Matter of 10 minutes

Resource optimization: From this…



Resource optimization: ...to this.



Current Design Status

- Completed
  - MGT DAQ
  - MGT Test Vectors
  - Gb Ethernet
  - PPC development application

- To-do
  - Finalize SLINK/ROD controller
  - LTP interface and BC clock
  - Finalize PPC application
  - Slight modification of pulse reconstruction

Thank you!