ITk Strips with 1MHz Readout

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Executive Summary

A feasible configuration for reading out at the L0 trigger rate: Star connected FE-ASICs on hybrid, packet building on HCC. HCC requests one event at a time from FE-ASICs - only one event per packet. Variable packet length, averaging ~250 bits data (= 250Mb/s @ 1MHz L0 readout). Implies 320Mb/s links from HCC to GBT with 2xGBT or 1x lpGBT per stave-side.

Introduction

The current (LoI) strips module design is optimised for relatively low occupancy. Each FE-ASIC, covering 256 strips, generates complete and self-describing packets of data. These packets are fixed length to reduce bit count and improve predictability for the readout system. Each packet comprises ~60% hit data – the rest being headers, L0ID etc. Although slightly wasteful of bandwidth, the format is robust, and neatly fits within the planned 1 GBT per stave-side.

Strips modules have up to four independent hybrids, each with their own readout link. Each hybrid FE-ASIC transfers data serially, sometimes via adjacent FE-ASICs to a hybrid controller chip (HCC). This makes efficient use of the data line routing on the hybrid.

As the expected pile-up/occupancies have increased, and trigger-rate options have reached 1MHz readout levels, bandwidth estimates exceed a single GBT. Furthermore L1Track is squeezing the latency of regional-data packets highlighting bottlenecks in the hybrid architecture. This has prompted a re-evaluation of the hybrid and chipset, the outcome being the “star hybrid” idea presented here.

This document details *first thoughts* on this new topology, and should not be considered a plan, statement of intent etc.

Star Hybrid

The current hybrid design has FE-ASICs connected in 2 chains of 5. Data flow is regulated using Xoff lines (to avoid overflowing small FIFOs) in the opposite direction to the data. Each chain can be readout from both ends (in case of dead chips). This adds up to 8 data lines per HCC on a barrel hybrid, and 10 on the worst-case end-cap hybrid.

As the name implies, in the star formation each FE-ASIC has its own point-to-point connection to the HCC. To keep the data line count down, the Xoff lines are removed and a request based system of flow control introduced (see the next section). The total number of data lines becomes 10 on the barrel, and 12 on the worst-case end-cap hybrid. This will likely lead to an extra layer in the hybrid flex circuit, but this will have a very small effect.

The current FE-ASIC (ABC130) transfers data to the HCC at 160Mb/s. With the star configuration the total BW into the HCC will become 1.6Gb/s. This is far greater than any envisaged stave link rate, but is advantageous as it allows the HCC to be filled fast and not require derandomising buffers, protecting against delays in waiting for very occupied FE-ASICs.

Trigger-Readout Flow

Without Xoff flow control, data is requested by the HCC from the FE-ASICs when needed. This means that L1 triggers are queued on the HCC until it is ready for data. The flow becomes:

- Receive L0 at HCC
- Generate L1 word and queue
- Send L1 to FE-ASICs
- Wait for all data for that event*
- Build packet (adding headers, L0ID, BCID, parity/markers etc.)
- Send to GBT

* To optimise the size of the HCC buffering required, it may be necessary to limit the number of hits sent by an FE-ASIC for a given L1 request. In this case the data could be tagged as incomplete and the HCC could resend the same L1 request (or a slightly modified one).

In this schema the FE-ASICs provide event buffering as they do now, and the HCC needs only to store ~3 events:

1) In-progress receiving
2) Packet building (or built)
3) In-progress sending

Data Format and Bandwidth

Simulation has been performed to estimate the number of hits per event at 200 pile-up. Presuming we maintain the current clustering algorithm - where data is transferred as a cluster with the strip address of a hit and a bit-map of the next 3 strips – we see the number of clusters per HCC per event in figure 1 below, for the busiest innermost short strip barrel layer HCC.

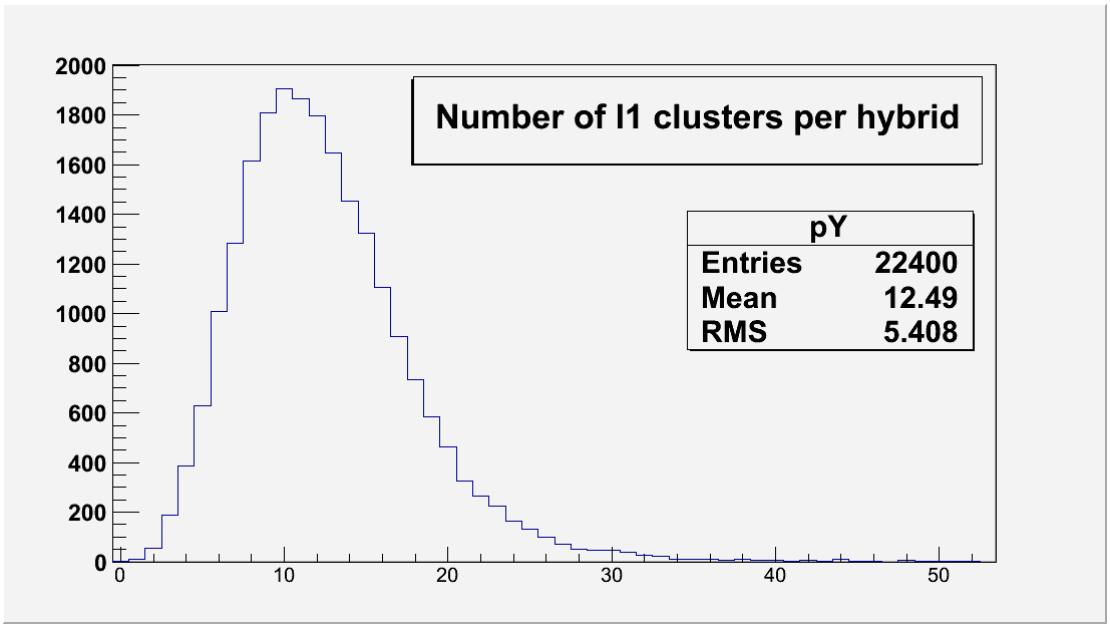

Figure 1. Number of clusters per event for a worst-case barrel hybrid

The average number of clusters for the worst-case barrel hybrid is around 13, but the wide range of values suggests that fixed length packets are not optimal in terms of bandwidth. This leads to a packet format (and length) as shown below (for example).

Bits	Description
3	Header/Trailer
8	L0ID
8	BCID
5	Type
6	Cluster count
8	ECC or parity and/or markers
195	195b – Hits (15b x 13)
233	**TOTAL**

Figure 2. Example packet format

An average packet is 233 bits long, so at 1MHz L0 rate readout, we transfer data at 233Mb/s between HCC and GBT, for the worst-case barrel HCC (which is the closest to z=0 in the inner-most short strip layer). For the worst-case end-cap module this is 263Mb/s.

To improve predictability and DAQ resource optimisation, it is proposed that a cap on the number of clusters per packet be imposed. In these cases a second packet will be sent with the extra cluster. Looking at figure 1, a value of 31 seems reasonable.

Packets in this format are a much closer match to the proposed FELIX data format than the existing 64 bit format.

Latency (and the L1 trigger)

We expect to retain the region-of-interest based trigger functionality in a new chipset. This will not only provide flexibility (we may need to revert to 400kHz readout), but also ensure that event data reaches the L1Track system in time.

When reading out at L0, it is presumed that all of the data required by the L1 trigger will be available in the counting room and thus not an on-detector problem. This depends on being able to transfer all data from the FE-ASICs to the counting room (and on to the L1 trigger) within the L1 latency. Simulation will be needed to see if peaks in trigger rate and occupancy will substantially delay data.

If this is the case, the R3 signal could still be used to extract data early: the HCC would maintain two queues - one for L1 and the other for R3. R3s would have priority: R3 data would be requested from the FE-ASICs and sent to the GBT before any L1 data.

Implications

To readout at a 1MHz L0, we need a 320Mb/s link for each HCC. Although tests have shown 320Mb/s is likely feasible on 1.3m of Cu/Kapton, further studies are required.

On a stave-side we have 26 HCCs, requiring 8.3Gb/s total BW. This exceeds the BW of a single GBT (4.5Gb/s), so 2 GBTs or an lpGBT will be required per stave-side. End-caps have fewer HCCs.