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ITk Strips at Higher Rates

v0.01

Introduction

ATLAS Upgrade ITk Strips readout at higher rates affects many components and has cost and material implications. To assess feasibility of any changes, particularly when including their impact on physics, is complex.

This document will attempt to describe some of the factors involved and what we know so far. There will likely be many more to add, and outstanding questions, incorrect assumptions, wrong information and possibly even provocative statements – everything here is open to discussion!

The strip tracker made of staves in the barrel and petals in the endcap. Petal development is behind stave development (for better or worse) with the configuration still evolving. As such we will talk more of staves here, presuming that this can be mapped on the petals in some way.

Our readout is primarily constrained by the bandwidth (BW) of the data links connecting the various components between the silicon sensor and the counting-room. In general, lower rates are better as they equate to less power and material, but these come at the cost of, for example, more complex (and larger) front-end ASICs. We need to find a balance.

There are many interleaved constraints, including bandwidth, latency, cooling, material and physics and cost. Ultimately a good simulation of *everything* is needed, but this is both difficult and time consuming: we need to be clear on what needs to be simulated in the first place. This document hopes to address at least some of these issues.

General Readout Schema

The baseline architecture from the LoI has a 2 level trigger plus regional readout (R3), with rates as follows:

- L0: 500kHz
- L1: 200kHz
- R3: 50 kHz (10% of L0 rate)

The rational is to reduce BW and increase time for a trigger decision buy storing data on the on the FE ASIC during trigger processing. This is achieved via the 2 level trigger – the first - level-0 (L0) - copies event data from a pipeline to a buffer, storing it in a memory addressed by its level-0-ID (L0ID). The second trigger – level-1 (L1) – initiates readout.
The L1 trigger is a small message than includes the L0ID of the event to readout. As such it is asynchronous and these L1 “requests” can be queued on the front-end ASIC.

An additional feature allows event data to be readout after L0, but before the L1. This allows some data to be used in the L1 decision. This readout is initiated by a Regional-Readout-Request (R3) and, like the L1, is a small message containing the L0ID of the data of interest. The R3 message can be targeted at a subset of all modules, and is expected to only affect 10% thereof.

A scenario for higher rate readout is doubles these numbers to: L0/L1/R3: 1000/400/100 kHz.

An alternative approach is to readout everything at L0. This effectively moves the L1 buffer to the counting room. This will still allow the L1 trigger to request data from regions but this will happen in the counting-room, and is therefore beyond the scope this document.

Bandwidth

Increasing the trigger rates is all about the bandwidth limitations across the system. We need to look at occupancy in the sensor being converted into hits in the ABCs, and follow the data through the system to the counting room.

Regardless of the triggering scenario, event data needs to flow though the same chain of hardware:
- FE ASIC (ABC130)
- Hybrid and Hybrid Controller (HCC)
- Stave/petal links (HCC to GBT, electrical)
- Off-detector links (GBT to counting room, fibre)

Calculation of BW uses the strip hit occupancy per bunch-crossing and the ABC130 fixed length packet format to produce a packets-per-chip-per-event number for various pile-up levels.

Using an approximate simulation, where min-bias events are added together to achieve the desired pile-up, the numbers for packets/chip/event are shown below (these need to be rechecked with full simulation and current geometries).

With 64 bits/packet and 10 ABCs on a hybrid, we can get an estimation of the BW required for various trigger rates in the inner-most barrel in the table below. Endcap numbers are currently 40-50% higher on modules with higher chip counts.

For the RoI based schema there are 2 data generating triggers: L1 and R3. The R3 rate is expected to be 10% of the L0 rate (10% of 1MHz). Ignoring that R3 data volume is a little lower than the L1 data volume, for the LoI x2 schema we have a combined trigger rate of 500kHz.

Pile-up:	100	200	300
Packets/chip/event	0.37	0.65	0.88
HCC BW at 200kHz L1	59Mb	104Mb	141Mb
HCC BW at 500kHz L1	118Mb	208Mb	282Mb
HCC BW 1000kHz L1*	236Mb	416Mb	563Mb

Table. BW for strips inner barrel (the endcap could be 50% more)
* Equivalent to readout at L0

Latency

Closely coupled to the bandwidth is the latency of regional data (R3-data). It is affected by the saturation level of the links, and starts to increase well before we reach absolute BW limits.

The Muon sub-systems will have great difficulty changing some of their front-end electronics. In this configuration their (L1) latency limit is 30us. This increases the time pressure on the trigger to make a decision. Using the regional data can help make tracking based decisions, but adds to the latency problem.

Calculating the latency limits requires a discrete event simulation – where the whole system performance is modelled over time. This has been done using the same occupancy numbers used above and shows R3-data latency starting to increase exponentially when the BW is about 60% of the maximum available. This implies we need to double the BW!

Alternatively, reading out at the L0 rate does not have the constraints of R3 latency, but data will still need to get to the counting room in time to inform the L1 trigger decision (within 15-20us). We are expected to cope with instantaneous trigger rates of up to 40MHz for short periods of time – this could well delay data to beyond the latency limit.
[NOTE: this could be the VERY good reason why L0 rate readout with the Muon latency constraint is not possible].

An improved system will need to maximally prioritise R3-data. This will likely require a re-design of the connections between ABC and HCC.

It's worth mentioning that without the Muon constraint, all the other sub-detectors have the opportunity to increase pipeline and buffer lengths. The ABC130 can store data for more than 200us at a 1MHz L0 rate. This opens up different options for the trigger. What will we be able to do with the extra 150us? Will we be able to *reduce* the L1 rate? Is a 1-2MHz L0 with a 100MHz L1 a better solution?

Material and Cooling

In most cases increased trigger rate leads to increased material and heat on-detector. This is seen as a bad thing.

The ABC130 requires a factor of 4 less power than the ABCN. This has dropped the cooling requirement to the level where the structural requirements of the cooling infrastructure are the dominant drivers (*** there must be a better way to write this). In other words, we can't make the cooling pipes smaller, or they will collapse.

Increased readout on the stave will likely require more copper traces on the the Kapton (2 links per HCC) – the feasibility of this and the effect on material needs to be evaluated.

At the end of stave, increases in BW equate to twice the number of GBTs, and heat. Even with lpGBT operating at twice the BW and half the power, for the L0 readout option we would need 2 per side. But if we have excess cooling, this may not be a problem.

So what about the extra material at the end of stave – it can be argued that, in many cases, this region does not affect tracking as there is little sensor area in the shadow to the barrel end-of-structure. The endcap EoSs are on the edge of the tracker volume.

Simulation is needed here!

Implications on the Hardware

The increased rates scenarios cover a few have a range of factors, detailed below.

	Baseline (LoI)	**LoI x2**	**L0 Readout**
L0 rate	500kHz	1000kHz	1000kHz
L1 rate	200kHz	400kHz	n/a
R3 rate	50kHz	100kHz	n/a
FE pipeline	6.4us	10us	10us
L1 buffer	25us	60us	60us
Deadtime	2BC	1BC(?)	0BC

Increasing rates beyond the baseline requires changes to the design of the tracker. Each component has different challenges. In general LoI x2 doubles all rates, and the L0 readout option doubles them again. In almost all cases the hardware cannot do the same without modification.

ABC130 ASIC

The ABC130 is designed to readout at 160Mb – more than enough BW, but this is divided by 5 (or 6 on the endcap) as chips are in chains. This means that the ABC130 was designed to generate <30Mb of data.

At 500kHz triggering, 2 chains of 5 chips still have enough BW. For higher rates the chains will need to be shortened and multiplied – adding more links to the HCC (star like configuration). Conveniently the current configuration has redundant links that allow shorter chains, even on the current hybrid design with the baseline HCC design.

As the ABC130 was designed for a 200kHz trigger, the packet building logic uses a power efficient, serialised method to build packets – this restricts the L1 rate to around 300kHz (*** needs checking). Future implementations will need a parallelised packet builder.

The ABC130 has a pipeline of 6.4us, but his can likely be extended (especially if the L1 buffer size can be reduced to free up space, if required) The ABC130 has a large L1 buffer that can hold >200us of data (at 1MHz L0). L0 deadtime is currently 2BC, but this can almost certainly be improved in an updated design.

To be able to readout at 1MHz, the ABC130 will need a much faster packetiser – 1us *average* – ideally <400ns to accommodate bursts and fit with packet transfer time.

HCC ASIC (and Hybrid)

The HCC has 4x 160Mb inputs connected to two chains of ABCs. This is sufficient raw BW for all of the scenarios discussed in this document. but the R3-data latency is still a problem.

To reduce R3-data latency the HCC will need to apply prioritisation to incoming ABC packets based on type. To overcome queuing problems in the chain, a star configuration is preferred. Here each ABC has a dedicated link to the HCC, allowing R3-data to always be transferred from the ABC with priority.

The HCC can transfer data on the stave at 320Mb. To cater for higher rates, 2 links are a possible addition to the design.

Stave/Petal Links

These cover the links between the HCC and GBT (located at the End-of-structure. They vary in length from about 0.1m to 1.4m. These are a SLVS differential Cu/Kapton flex-circuit. The baseline (LoI) system operates these at 160Mb. To achieve higher rates a number of items need to be confirmed feasible:

1. 320Mb on the 1.4m SLVS lCu/Kapton. Some tests were done a few years ago but these would need to be repeated more rigorously.
2. 640Mb operation can be looked at, but will likely require 2 320Mb links – the stave tape design need to check if this fits.

3. To operate with 320Mb stave links, we need 2 GBTs (or 1 lpGBT), and double that for the L0 rate readout. On the presumption that the extra material, power, complexity and cost of having 2 (or 4) GBTs per stave(petal)/side is not desirable, this option hinges on successful production of the lpGBT at CERN on the right timescale.
4. We also assume that we can turn-off the FEC for the data links (although this assumption looks very plausible).

Idea: can the shorter links run at 640Mb?

Some (more) questions

- What are the real limits (with margin) for the rates (and pile-up)
- Trigger structure in time - 1MHz and bursts – what are the limits?
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(My) Conclusion

In general the LoI x2 option seems possible, but needs confirmation from simulation and the link tests.

If Muons don't change their hardware, I doubt 1MHz readout will be possible, as latencies will be too high during trigger bursts.

If Muons are able to change their hardware, and we can get the lpGBT, *and* we can squeeze all the links onto the stave, it is possible.

But why not save all the bother, and use the extra latency (>150us!) to allow the L1 trigger more time to reject more events. Why not have a 2MHz L0 and 100kHz L1 (with a 200kHz R3)