BCC
Buffer Control Chip

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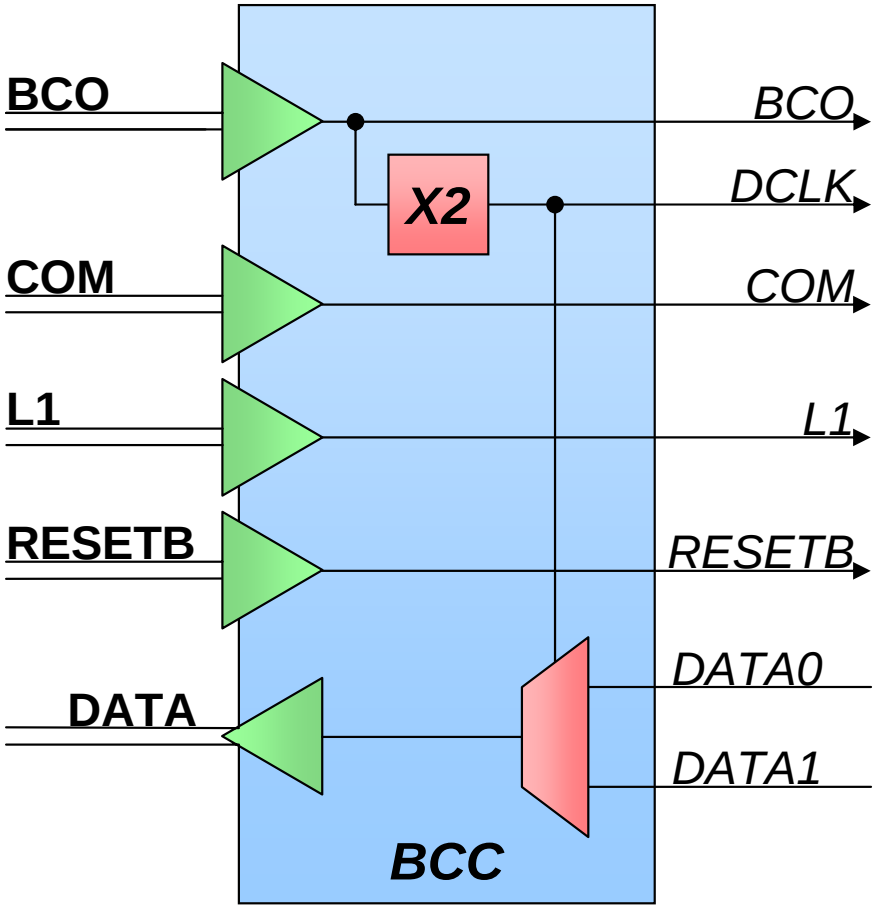
Introduction

- The BCC is an ASIC for interfacing ABCNs on a hybrid to a stave.
- Born out of an opportunity to use ‘spare’ silicon on the edge of a wafer for a run of a larger chips (KPIX) and availability of expertise from SLAC.
- Quick turn around = lots of hard work!
- Manufacture by TSMC, through MOSIS
  - 0.25um process.
  - Submission is March 30, 2009, expecting a 3 month turn-around



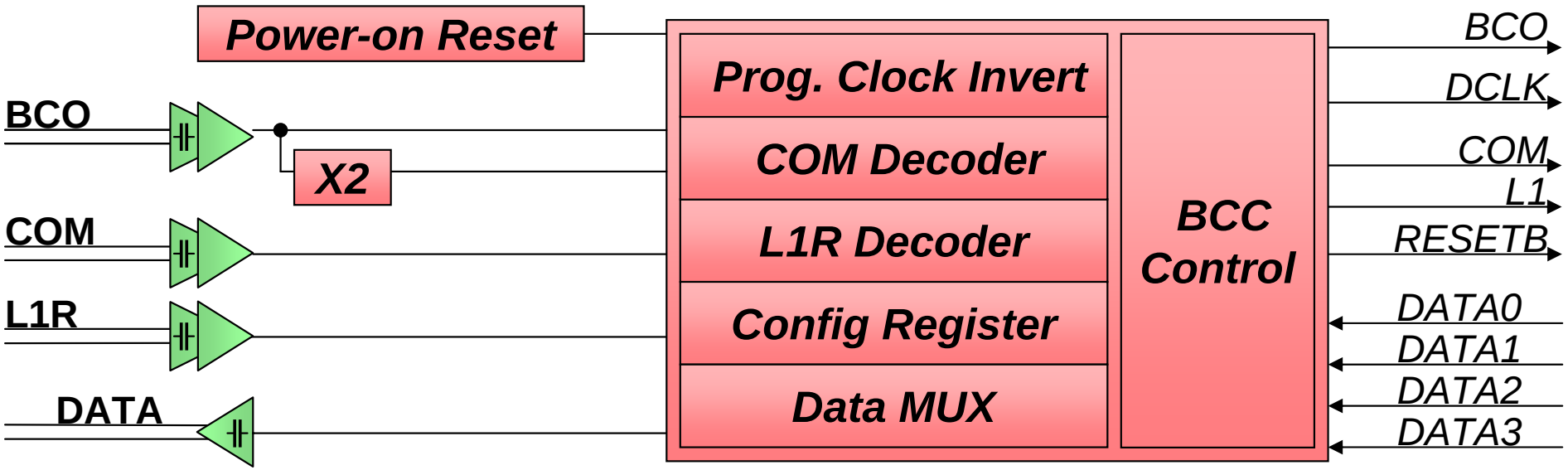
Was planned to be a very simple chip:

- LVDS stave to ABCN single-ended
- Clock multiplier for 80MHz readout
- MUX to combine 2 columns of data

BUT then we started adding things…

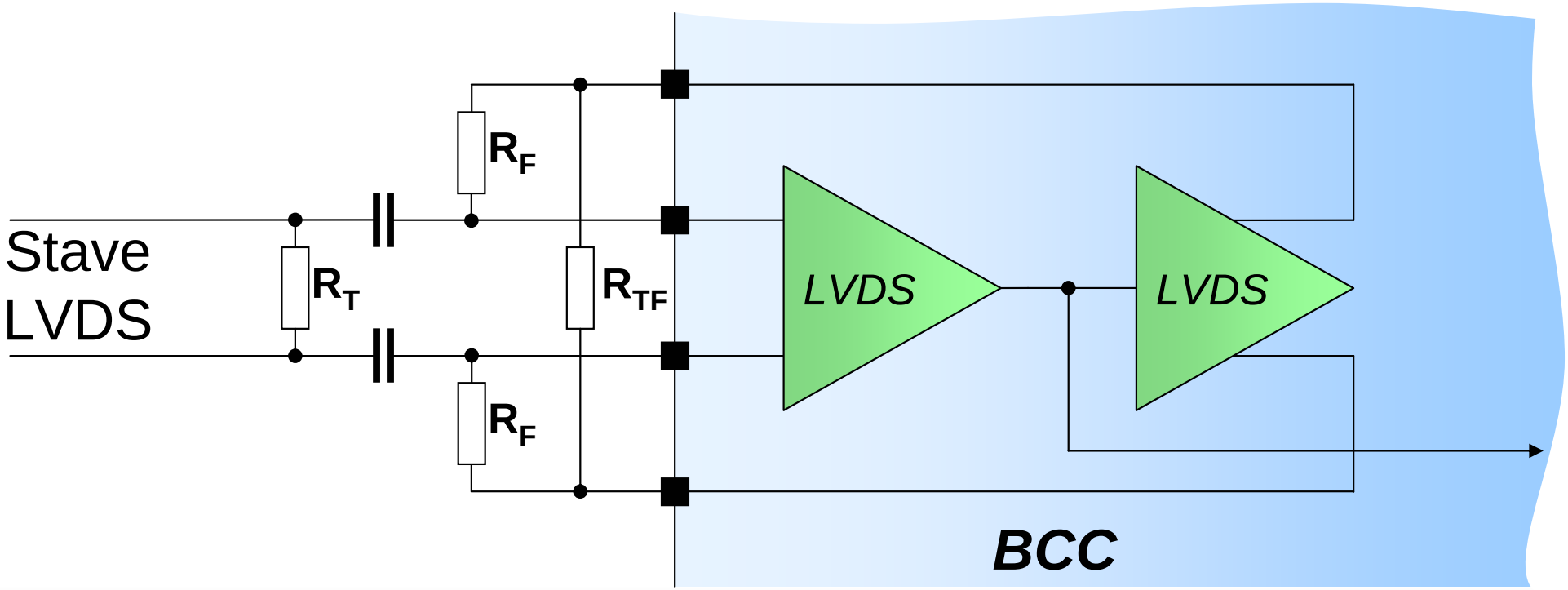
BCC Features

- Special LVDS buffering – DC signalling, AC coupled, DC out
- 40MHz BCO multiply to 80MHz clock
- ABCN data clock (DCLK) selectable as 40 or 80MHz
- Multiplex 2 ABCN streams onto 80/160MHz data line
- L1 line multiplexed with RESETB (L1R) – separate decoder, provides BCC-RESET
- Programmable Clocks inversion
- ABCN data sync (“sample and hold”) (invertible)
- ABCN signals synchronised to BCO (invertible)
- Redundant ABCN data lines selectable
- BCC config register, with read-back
- Power-on Reset

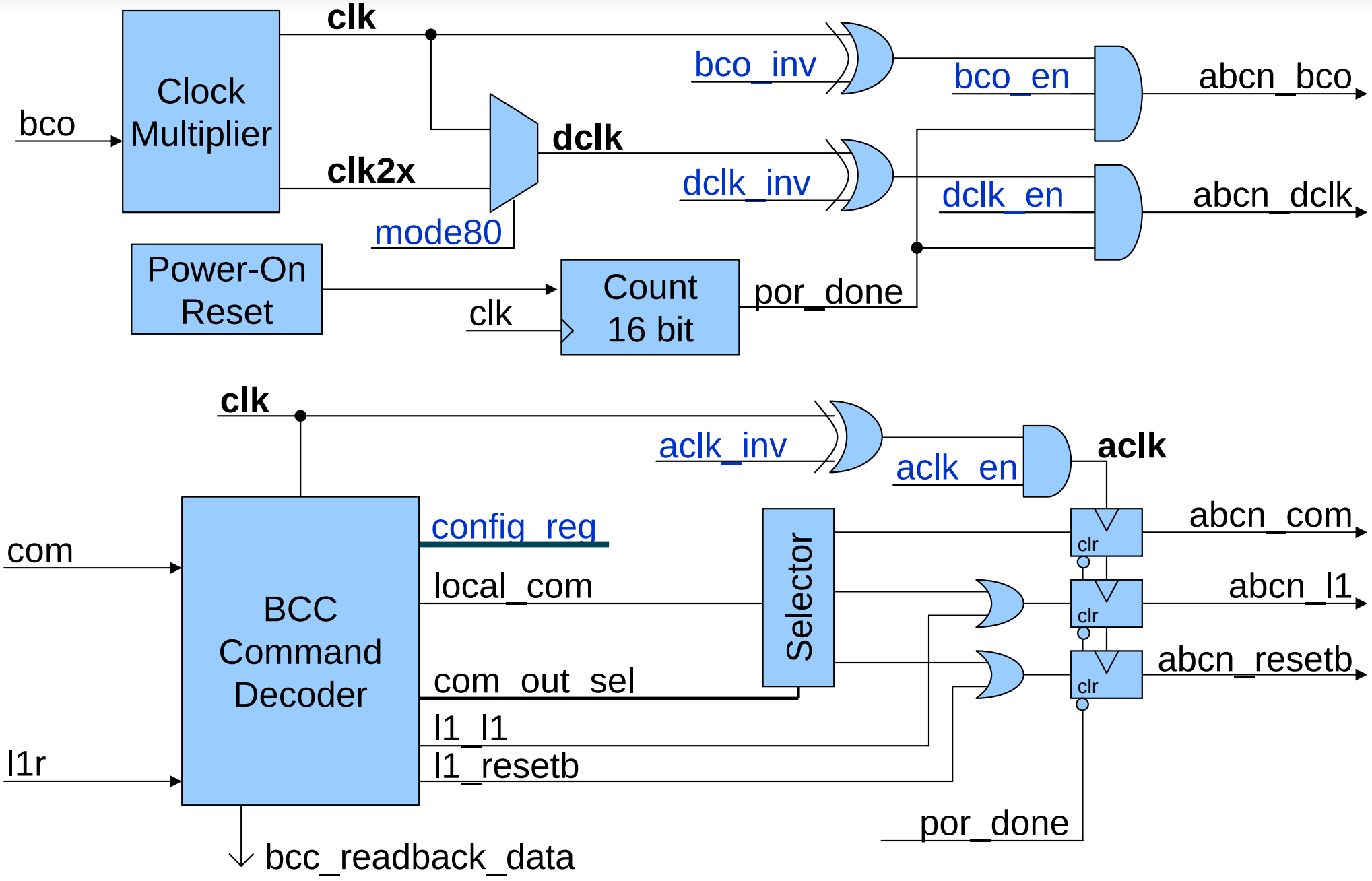


'Special' LVDS DC-AC-DC Buffer

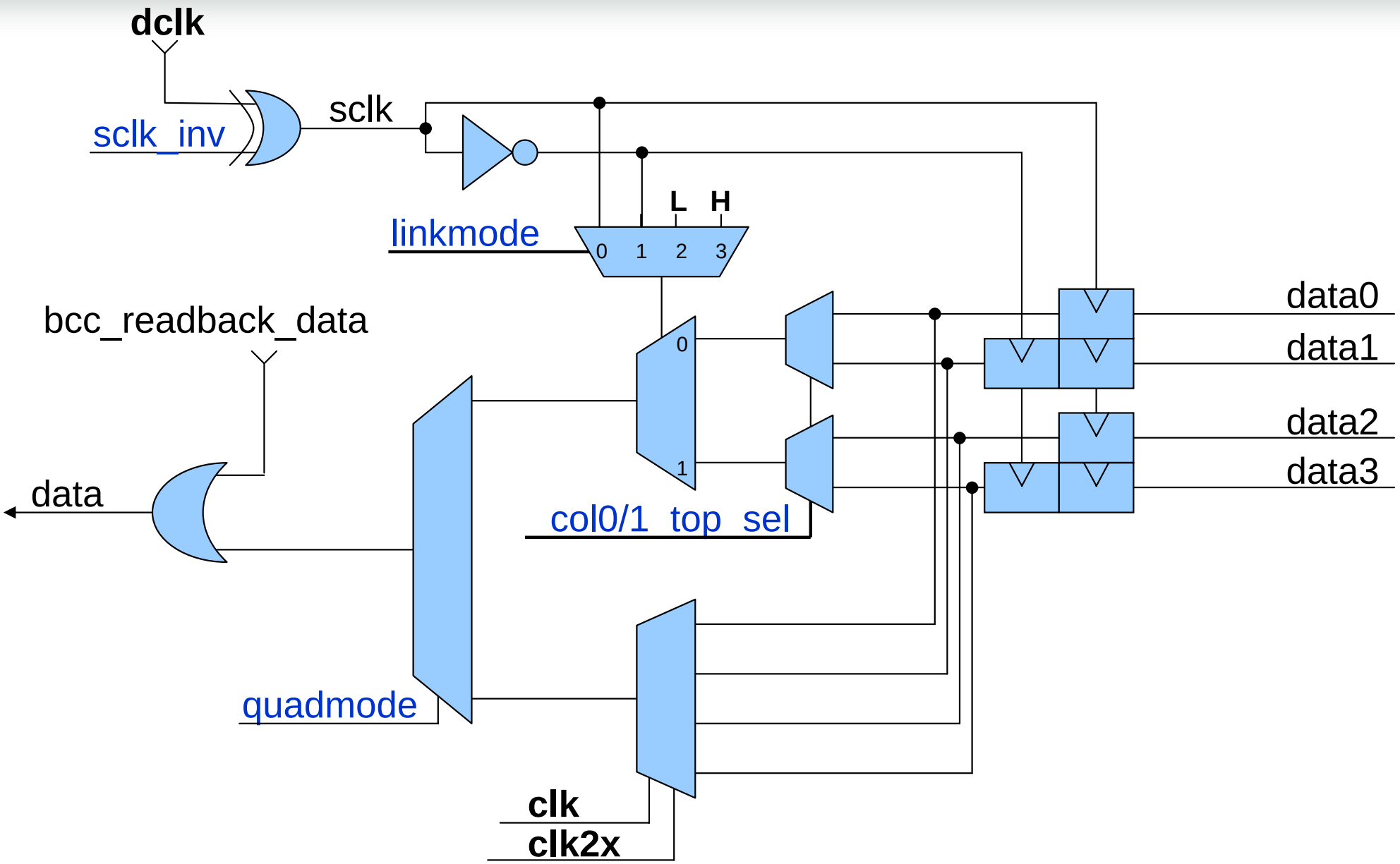
- DC Signals are AC coupled
- Feedback is used to 'hold' the level beyond the RC constant
- Passives are external to BCC for tuning
- RF in particular is dependent on data-rate and final chip characteristics



Schematic I (to ABCN)



Schematic II (from ABCN)



COM/L1R Command decoding

The BCC intercepts the COM and L1R lines.

- Leader/Command-type it detected
- Fast commands are forwarded to ABCN (with 4 clocks latency)
- Local commands/data extracted

L1R:

- `X100` issue “100” on L1 lines
- `X110` issue “110” on L1 lines
- `1110` issue “111” on ABCN_RESET line
- `1111` internal BCC soft-reset (clocks and config register unaffected)

COM Leader:

- `110` Broadcast L1 - forward to ABCN
- `101CCCC` Broadcast fast-command - forward to ABCN
- `111` BCC specific, details on next slide

COM Data Format

BCC Addressed Transfer	111 AAAAAA TTT LLLLLLLLLLLLLLL DDDDDDD...DDDDD
1) Send Data on ABC Com	000 LLLLLLLLLLLLLLL DDDDDDD...DDDDD
2) Send Data on ABC L1	001 LLLLLLLLLLLLLLL DDDDDDD...DDDDD
3) Send Data on ABC Reset	010 LLLLLLLLLLLLLLL DDDDDDD...DDDDD
4) Write BCC Config Reg	101 RRRRRRRRRRRRRRR
5) Readback BCC Config Reg	100 (returns 100RRRRRRRRRRRRR1)
6) Read BCC ID Reg	111 (returns 10000000000AAAAAA1)

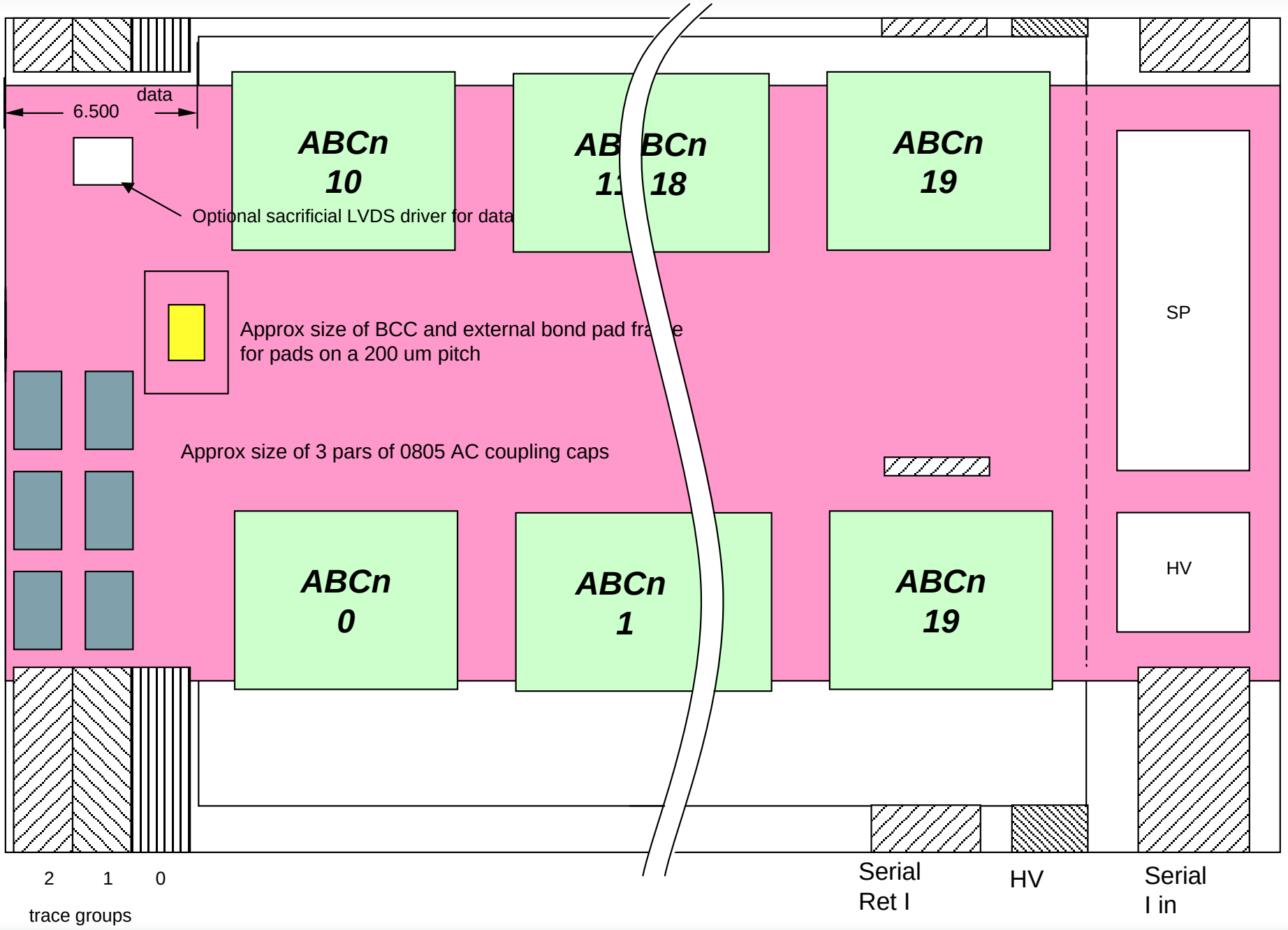
- **A: Address** (6b) BCC target ID
  - 111111b is used to broadcast to all BCCs
- **T: Type** (3b) data destination
  - MSb = internal to BCC.
- **L: Length** (16b) specifies bits to wait before returning to leader detection
  - Note: the BCC will wait the specified length of time even if not addressed – this ensures it will not start leader detection mid transfer to a different BCC.
- **R: Register** (16b) contains 16bits BCC config reg, padded to 16 bits
- **D: Data** – Sent to ABCNs, length should be in L field.

BCC Config Register

BCC Config Register bits:

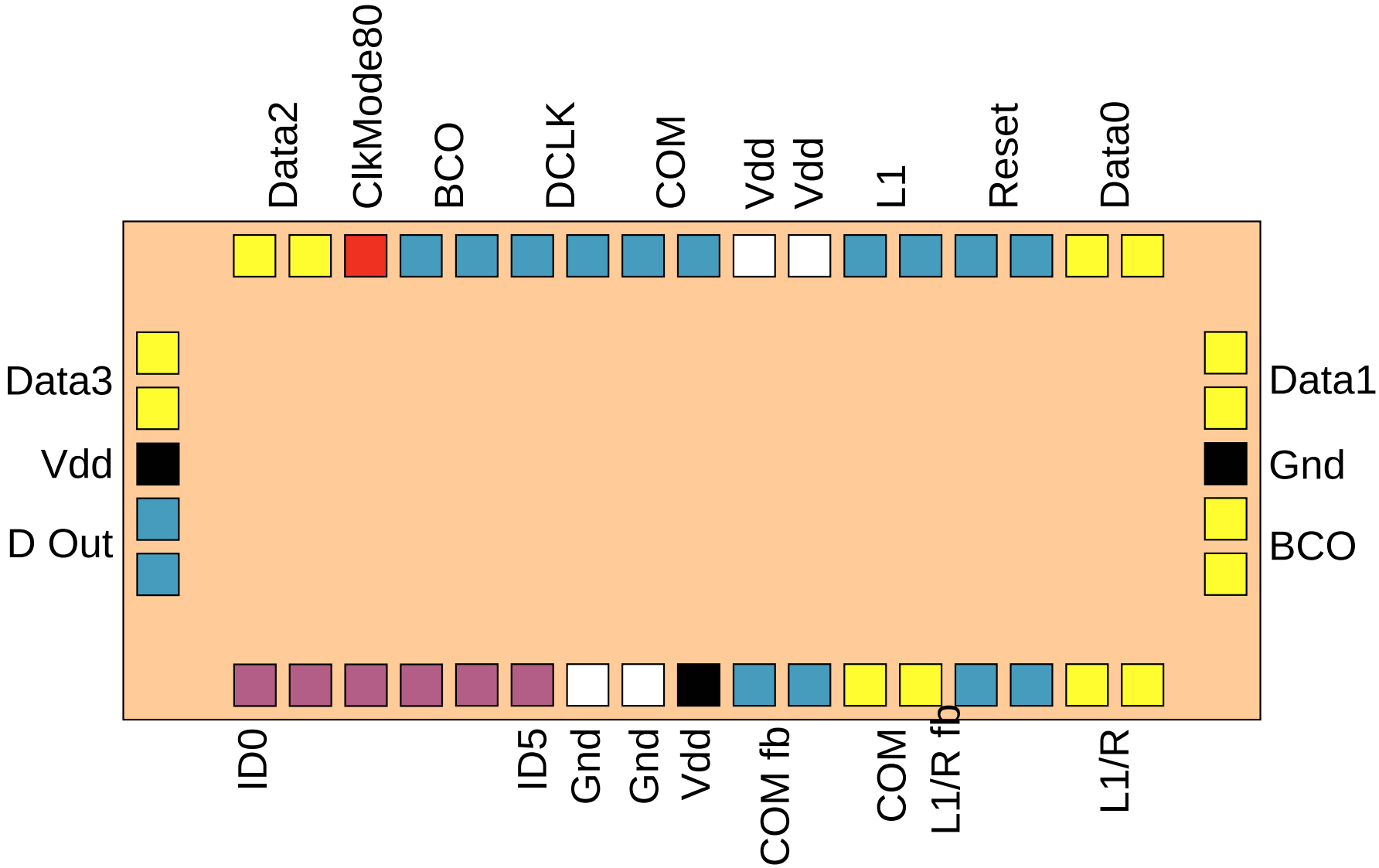
12) Column1 top ASIC data select
11) Column1 top ASIC data select
10) ABCN DCLK enable (*set at reset)
9) ABCN BCO enable (*set at reset)
8) ACLK enable (ABCN signals-sync clock enable) (*set at reset)
7) ABCN DCLK invert
6) ABCN BCO invert
5) ACLK invert
4) SCLK invert (clock used to sample ABCN data)
3) 80Mhz readout mode select
2) Quad Mode select
(1:0) Data MUX select source
00: DCLK
01: NOT DCLK
10: 0 (select DATA0/2 only)
11: 1 (select DATA1/3 only)

BCC on Hybrid



Pad Layout

- Pitch?
- Double row of pads?



BCC Status/Conclusion

- All components are designed:
  - LVDS receivers & drivers
  - Clock multiplier
  - Power-on reset
- Initial layout done
- Things yet to do
  - All components needs simulation
  - Digital core written, but needs tweaking
  - More simulation of digital behaviour
  - Hand route components
  - Simulate entire BCC
  - LVS entire BCC
  - DRC entire BCC

BCC Layout Feb 10, 2009

- Size = 2.3mm x 1.1 mm
- 42 pads May increase by two on sides
- 9 LVDS Receivers
- 8 LVDS drivers
- 90 mW – LVDS drivers