Notes on 01 December 2010

Proposition for data readout (source document Data-Format-packet.pdf)

HEADER

Header	**1**	**1 bit generated by MC**
Hybrid_ID 5 bits 24 hybrids per half single sided stave	**Binary order**	**5 bits generated by MC** **Avoid null and all at one**
Chip_ID 4 bits 10 ABCn per hybrid 1 (2) MC per hybrid	**Binary order**	**0 and 1 reserved** **3 to 12 for ABCN** **13, 14 for MC**
ERC code	1	1bit generated by MC
Data_Type 3 bits L1 data, L0 data, registers, etc.	**000** **001** **110** **010** **100** **101** **011** **111**	Error code ? L0 Data L1 Data Register data (any, incl. status) Slow Control Data Internal Data (self generated) Test Data Reserved
Global (chip) status code	1	Requires status examination
FIFO status	1	Near full FIFO
L0ID or Register Address 8 bits Should be large enough to cover the L1 latency. Assumed 1MHz L0 rate, 256μs latency	**Binary order**	**L0ID only for L0/L1 Data** **(this field could be moved to L0/1 data packet) or else Register Address (covers Status DCS Self Test) if non L0/L1**
BCID 8 bits 12 would be safer but 8 are sufficient as it is used in conjonction with L0ID	**Binary order**	**Irrelevant for non L0 Data ?** **"Empty" or used as checker field for L1 and Registers Data Type**
Total		
32 bits		

DATA PACKET

Strip_ID	**8**	**First Channel Address**
BC n-1 n n+1 for Strip_ID	**3**	
BC n-1 n n+1 for Strip_ID+1	3	
BC n-1 n n+1 for Strip_ID+2	3	
BC n-1 n n+1 for Strip_ID+3	3	
(ERC	**1)**	
Total		
20 (21) bits		

OTHER PACKET (NON DATA)

Status indicators	**4**	**Various status bits**
Content	**16**	**Register Payload**
(ERC	**1)**	
Total		
20 (21) bits		

Total 53 bits (funny number … it is a prime number)