3.4.3 Off-detector hardware and data paths

3.4.3.1 Overall Design

The track trigger builds on the existing Level-1 Trigger architecture, in which a potentially interesting event is identified, and a signal synchronous with that event is sent to the detector front-end (FE) modules. The FE ASICs transfer the event data from their pipelines to a readout buffer where they are queued and sent off-detector.

For regional data readout, the process has two important differences:

- The trigger in this case is a regional-readout-request (R3) only, and is not broadcast to all FE modules. Instead it is sent only to the Inner Detector modules inside the RoI.
- Readout is minimally buffered — when an FE module receives an R3, it must return the data as fast as possible (with known latency) employing prioritised multiplexing or a separate data path.

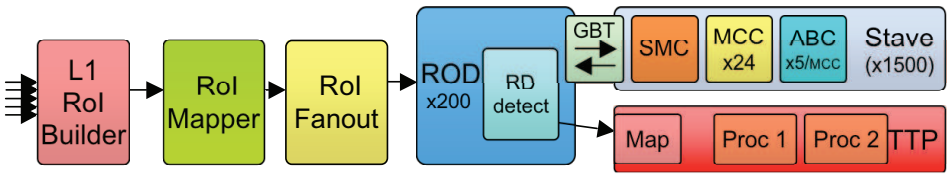

Figure 3.6: Overall system layout.

The Track Trigger process starts with the receipt of one or several RoIs from the L1Calo or L1Muon system by the Track Trigger RoIMapper (RoIM). This information is decoded and synchronised, generating readout requests to be sent to the modules within the RoI. At this stage the physical geometry of the detector is used to send R3 signal to the specific hardware chain connected to the desired FE module. The RoIM is described in detail below.

Using the topology of the current ATLAS SCT and Pixels, all FE modules are connected to off-detector Readout Drivers (RODs), so the RoIM will send groups of R3 signals identifying individual ROD channels. On each ROD, the R3 is integrated into the control link and sent to the stave. The SuperModule Controller (SMC) decodes the signal onto dedicated R3 signal lines connected to each module, identifying which should be read out.

The FE modules comprise a Module Control Chip (MCC) and many ABC FE ASICs. Upon receiving the R3, the MCC prepares for readout of track trigger data while forwarding the R3 signal to the ABCs. The ASICs process the event data and send it off-detector as fast as possible. In the case of dedicated track trigger links, these data would go directly to the Track Trigger Processor (TTP), otherwise they are identified on the ROD and forwarded on to the TTP.

3.4.3.2 RoIMapper design

The RoIMapper provides the hardware interface from the L1Calo and L1Muon Trigger systems to detector geometry-specific signals. It is tasked with three functions: interface to the L1Calo/Muon RoI system, map RoIs to physical module connections, and interface to the control system that drives the modules.

- Level-1 RoI Interface: The trigger system will probably send each RoI as a number giving the $\eta - \phi$ location and the type of RoI (which essentially defines the shape). These data will arrive at the RoIM as parallel data on a differential copper or a GBT (or similar) optical link. It is unclear whether each trigger subsystem will be connected separately or share a fibre/bus, but it will be necessary to time-align all RoIs for a given bunch-crossing. As the RoIM is at the top of the Track Trigger tree, it should also be able to function as a standalone R3 signal generator, using random or preloaded RoI information.

- RoI $\rightarrow$ Module map: The RoIM uses the RoI type and location to generate a list of target modules. Connection to these modules is via a channel on a ROD, so the module-stave-ROD mapping needs to be used. This needs to happen as fast as possible (< 25 ns), so the RoI-to-module mapping will be pre-loaded in RAMs, CAMs or associative memories. These could reside on an FPGA or in dedicated hardware — evaluation is needed. This system needs to be programmable to account for changes in layout or module-to-ROD mapping.

- ROD Interface: The RoIM sends signals to all the connected RODs in the system. As the final system could have ~ 3000 readout links (strips and pixels) connected to ~ 200 RODs, a fan-out system will be required. Additionally, the system must be synchronous, being able to fit all R3 information inside a 25 ns packet. Fan-out hardware will be needed and will be located in the ROD crate or next to the RoIM board. The distribution of lookup logic will to be optimised between RoIM, Master and Crate fanouts and RODs.

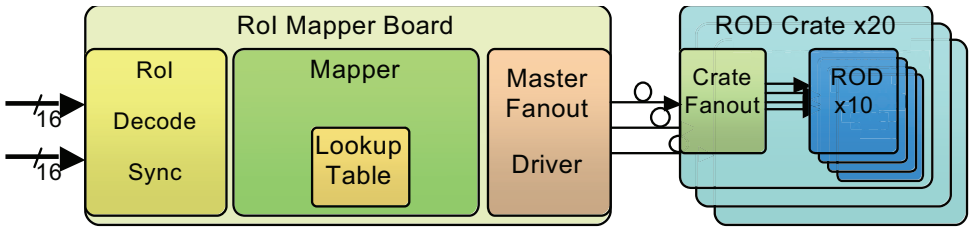

Figure 3.7: RoIMapper functional schematic.

3.4.3.3 RoIMapper Hardware Program

While requirements for a complete system required by the upgrade will be evaluated, it will only be possible to study a fraction of the system in hardware. Development will be consistent with larger system requirements, but scaled for bench testing. The use of RAM, ROM, CAM, or AM architectures will be investigated in FPGAs, with a view to understanding if ASICs are needed.

Construction of a demonstration system is planned. This will be integrated with the Tracker upgrade DAQ/Control prototype that ATLAS-UK plans to develop, as described in the tracker upgrade sections of this proposal. Depending on their availability, the early SMC prototype and modules will also be integrated.

Three units are required:

1. An RoIM development platform, using a high-power FPGA board with optical links. A good candidate is the ATLAS DAQ WP development board (HSIO), which is well known to the project.

2. An RoI generator (Level-1 RoI emulator), to generate signals simulating the Level-1 systems, to drive the RoIM. This could use a cheap development board or a subset of signals in the available on the HSIO.

3. An R3 Fan-out, to look at options for sending many R3s to multiple RODs. This could be a plug-in for HSIO, or use existing HSIO optical interfaces.

3.4.3.4 Track trigger processor

Although it is not proposed to build the Track Trigger processor (TTP) boards at this stage, it is important to understand the requirements for these boards and include them in the overall system specification. This work will be carried out in close connection with the pattern recognition studies, since the pattern recognition strategy influences and depends on the hardware technology on which it would be implemented. The aim of this task is to evaluate the alternative hardware choices for pattern recognition, including FPGAs, network search engines, and associative memory-based chips, and to specify the I/O requirements and interfaces of the TTPs to the rest of the system.

3.4.4 On-detector electronics and readout

The Level-1 Track Trigger relies on most other systems of the Tracker upgrade project integrating the required functionality. In this proposal, the tracker upgrade DAQ, Stave Interface (SMC), Tapes, Modules and Hybrid will all need to include aspects of L1Track. Additionally, it will be essential to work closely with the non-UK projects, particularly the MCC and ABC ASIC designs, as well as the CERN GBT/Versatile Link projects, to ensure that the required functionality for a track trigger is incorporated in these designs.

3.4.4.1 Stave Tapes Signal Distribution

Options will be investigated for distribution of regional-readout-request (R3) signals. To target a subset of modules/MCCs on a stave, ideally a separate line to each MCC is required. As stave resources are limited, investigations into trade-offs between increased numbers of control-links and higher transfer rates are needed. Regional data (RD) is more demanding in latency and synchronisation of stave readout resources than normal event data. It requires fast links which are always available. Merging this data into the existing readout architecture may be possible, and would probably be more efficient in terms of material and power. On the other hand, dedicated fast readout links would improve performance, which in turn could reduce the front-end pipelines and buffer resources and add efficiency there instead. These two alternatives will be evaluated in order to converge to the optimal solution.

3.4.4.2 End of Stave

Implementation of regional readout needs dedicated signals decoded from the control (optical) link. It is unclear whether this functionality will reside in the GBT hardware, SMC hardware or need additional components, but at the very least drivers will be needed for the regional-readout-request lines. In the opposite direction (data path) the option of dedicated regional-readout lines would require separate hardware either to multiplex into the existing optical link or to drive a second link. These issues need to be developed to understand better the additional needs.

3.4.4.3 Hybrid/Module

The hybrid has very tight constraints mainly due to its size. Any changes need to be carefully investigated. As the regional readout design advances, especially with respect to ABC ASIC, its integration with the hybrid must be considered. The implications of additional lines between the ASICs and the MCC as well as between the MCC and the tape need to be investigated. The feasibility and efficiency of the various design options will be studied. It is anticipated that a new hybrid prototype will need to be developed, and this has been included in the capital cost of the Track Trigger project.

3.4.4.4 DAQ (Off-Detector)

The prototype DAQ is tasked with reading out a large variety of hardware, from single-chip test boards to entire staves. As regional readout will be incorporated into some of these designs, the DAQ will need to be able to deal with both testing and co-existing with the system. This will include acting as a stand-in for SMC/GBT, and handling R3 command decoding and de-multiplexing.

The possibility of having dedicated regional-readout links from the MCCs means that the number of LVDS links being received by the DAQ could double. This needs to be factored into the DAQ design (probably requiring two HSIOs for stave testing).

Once off the detector, regional data needs to be split from event data and sent to a Track Trigger Processor (TTP). Although it is not planned to build a dedicated TTP in this bid, the use of the readout hardware as a test-bed for algorithms and for architecture evaluation would be beneficial.

As the DAQ will control or interface to trigger sources/generators, a regional-readout interface will also be needed.

3.4.4.5 ASICs

The Track Trigger requires support in the Module Controller Chip and ABC-X FE ASICs, although these developments are not UK projects. The UK work will include simulation studies into data compression, data formats and shared readout, and it is proposed to develop these into firmware as a possible contribution to the ASIC projects, and as a demonstrator.

- ABC: Regional readout introduces a new signal to the ASIC design. When an R3 is received, data must be copied from the pipeline and prepared for transmission. Dedicated signalling or “queue jump” logic are required to ensure the data leave the ASIC quickly.

To lower latency and bandwidth requirements, methods for reducing regional data volume on the chip will be investigated.

- MCC: The MCC passes data off detector from the ABCs via the stave tape and SMC. In the case of shared readout lines, it plays the important role of arbiter. It will also be responsible for adding headers, etc. to label the regional data. When an R3 is received by an MCC, a "hold" signal is sent to the FE ASICs, temporarily freezing normal readout. The regional data packet is then transferred from the ASICs with the requisite header and trailer, and then normal readout resumed.

3.5 High-Level Triggers

3.5.1 Background

The HLT comprises the hardware and software of the HLT farms (Level-2 and Event Filter) and the dataflow system. The farms consist of a total of some 2300 PCs running the trigger selection software. The dataflow system includes the Readout System (ROS), Event Builder, and network infrastructure. The ROS stores event data in Readout Buffers (ROB) pending a Level-2 decision, and serves the data to the Level-2 processors and Event Builder. The Event Builder assembles the data fragments, for events accepted by Level-2, prior to processing by the Event Filter and, for events passing the trigger, subsequent output to storage.

The ATLAS-UK HLT groups have played a leading role in designing, building and commissioning the HLT hardware and developing the event-selection software. All the construction-phase deliverables of the ATLAS-UK HLT project were completed on time and were in full use at the LHC start-up, as well as in the combined cosmic runs of the last quarter of 2008 and summer 2009. ATLAS-UK led the design, production, installation and commissioning of the ROB-in boards that physically implement the ROBs. Half of the 700 boards were manufactured and tested in the UK. The UK also played a significant part in developing the ROS software, which handles data requests and data movement within the ROS PCs. The UK contributed to the purchase of the PCs for the HLT processor farms and the TDAQ network equipment, having significant input to the specification and procurement of all these commercial hardware items, and currently provides the TDAQ resource coordinator responsible for these procurements.

The UK has made a major contribution to the Event Selection software, providing leadership in the areas of HLT track reconstruction, core HLT software, and electron and B-physics trigger selections, as well as providing overall coordination of the work on trigger selection algorithms. The UK provides the current Trigger coordinator. For Level-2 tracking, the UK has developed all the components of the Level-2 tracking chain, from data preparation to pattern recognition and track fitting, as well as fast secondary vertex reconstruction. For Event Filter tracking, the UK was largely in charge of developing the wrapper tools for embedding the offline tracking code in the HLT framework. In addition, the UK has led the work for developing the online monitoring tools and the validation tools for both the Level-2 and Event Filter tracking. The UK played a leading role in the design of the core HLT software, including the Trigger steering software. This component controls the running of the trigger algorithms in step-wise processing chains, which are configured so as to implement the trigger menu, and forms the trigger decision. Other key components of the core HLT software, developed in the